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(RESEARCH ARTICLE)

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Optimization of SMT process parameter for yield improvement of PCBS

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Abstract

The manufacturing process of Electronics Assembly has undergone a sea changes. Component industry has migrated to surface mounted devices from through whole components. This change has resulted into miniaturization of the equipment as well as pushed entire assembly operation to automatic process. Thus correct setting of process parameter is essential to maintain quality and throughput of the entire process. Process parameter need to be set as accurate as possible, so that there is no possibility any rejection.

Keywords: Surface mounted technology; Digital Voice and Video Recorder; Printed circuit board; Automatic Optical Inspection.

1. Introduction

The Digital Voice and Video Recorder (DVVR) system is designed to record voice communications. DVVR provides solution to record and replay the scenario for later training and analysis. The manufacturing process of the equipment is shown in Figure 1.

The equipment is checked thoroughly for meeting specification parameters during testing stages. The equipment is subjected for checking of various electrical parameter to ascertain performance during actual usages. Process mapping {1] is shown in Figure 2.

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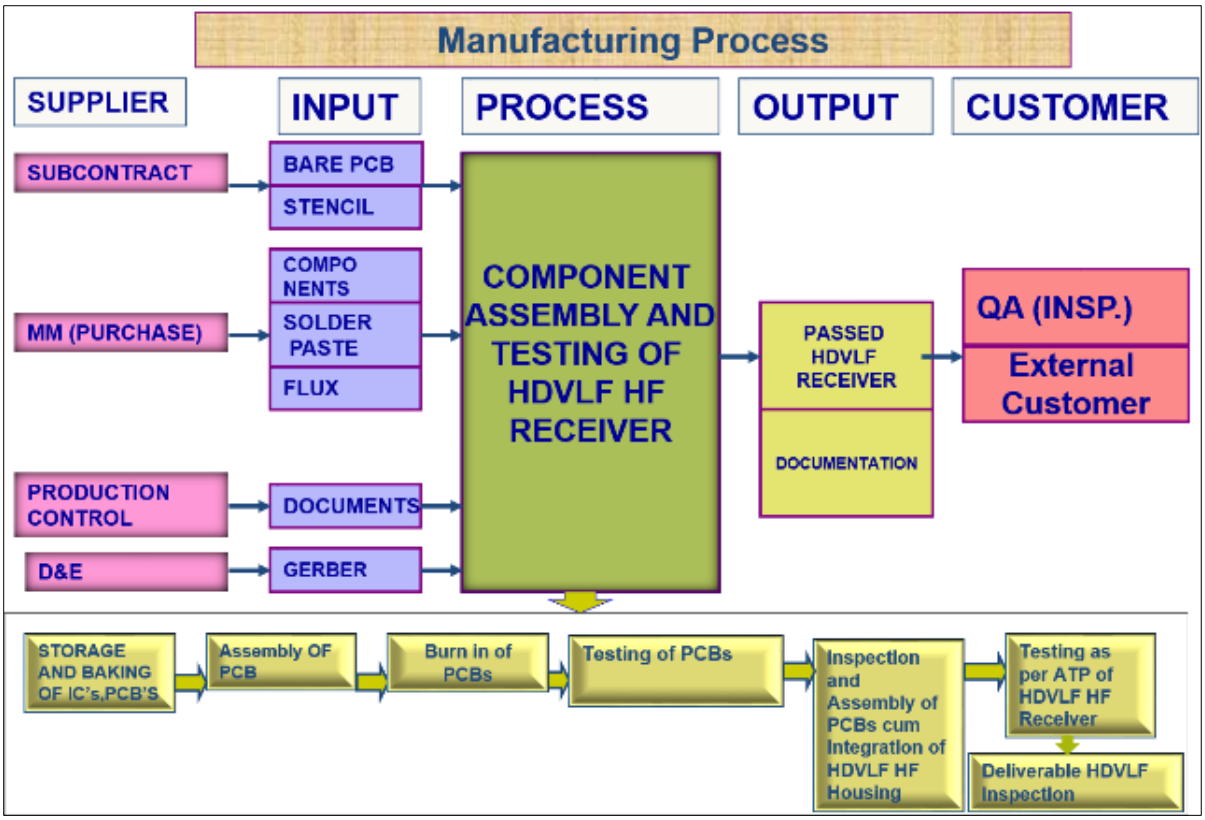


Figure 1 Manufacturing Process

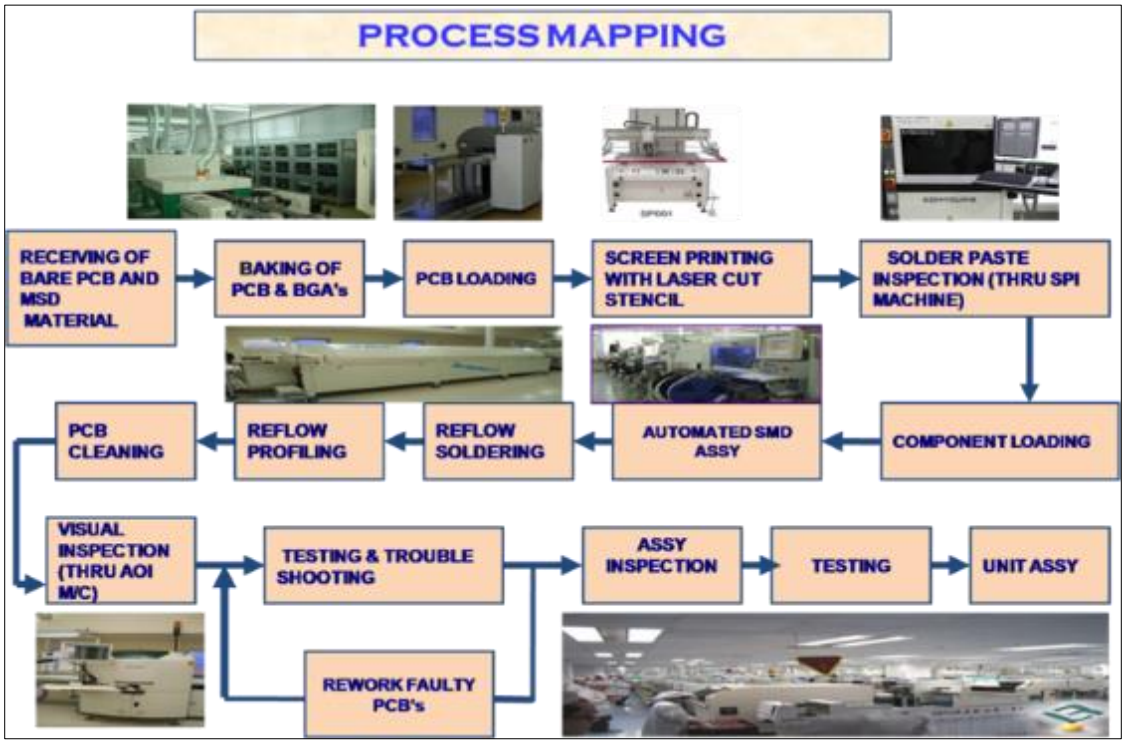


Figure 2 Process mapping diagram

2. Problem

During assembly process, following observations were noticed;

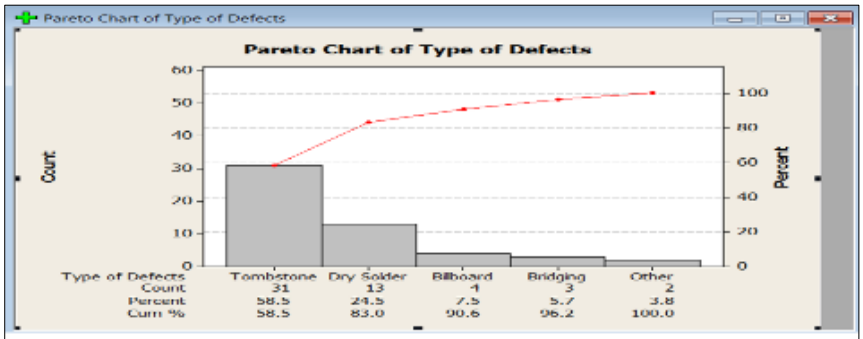
First time 0201 smallest size components (size- 0.5*0.25mm) were used in SOM card of DVVR in bottom & top side. Being smallest size of component, lots of challenges were faced during pcb assembly process & many soldering defects were identified during assembly & remain unattended. Defects were identified during functional testing of 20 nos. pcb lot which lead to poor first time pass at testing stage which is shown in Figure 3.

Hence it was decided to find out the root cause & carry out all necessary improvements in the process to minimize the defects rate in 0201 components so that yield of these pcbs can be improved .

MEASUREMENT OF INITIAL DATA AT TESTING LEVEL (FEB'2020) FOR 20 Nos. LOT	
Defectives Vs Defects	
PCB tested	20
No. of Defectives Troubleshooted	7
No. of Defects in PCB's	53
Pending for troubleshooting (Beyond repair)	1
First Time Pass	12
FTP%	60%

Figure 3 Measurement Data

The fault were analysed in Pareto chart[2] which is shown in Figure 4.



Type of Fault	Tombstone	Dry Solder	Billboard	Shorting (Bridging)	Shift
No. of Defects	31	13	4	3	2
% of Fault	58.5%	24.5%	7.50%	5.7%	3.8%
Cum %	58.5%	83%	90.6%	96.20%	100%

Figure 4 Pareto Chart

3. Analysis

Fault wise root cause analysis was done. Cause and effect diagram[3] of the process is shown in Figure 5.

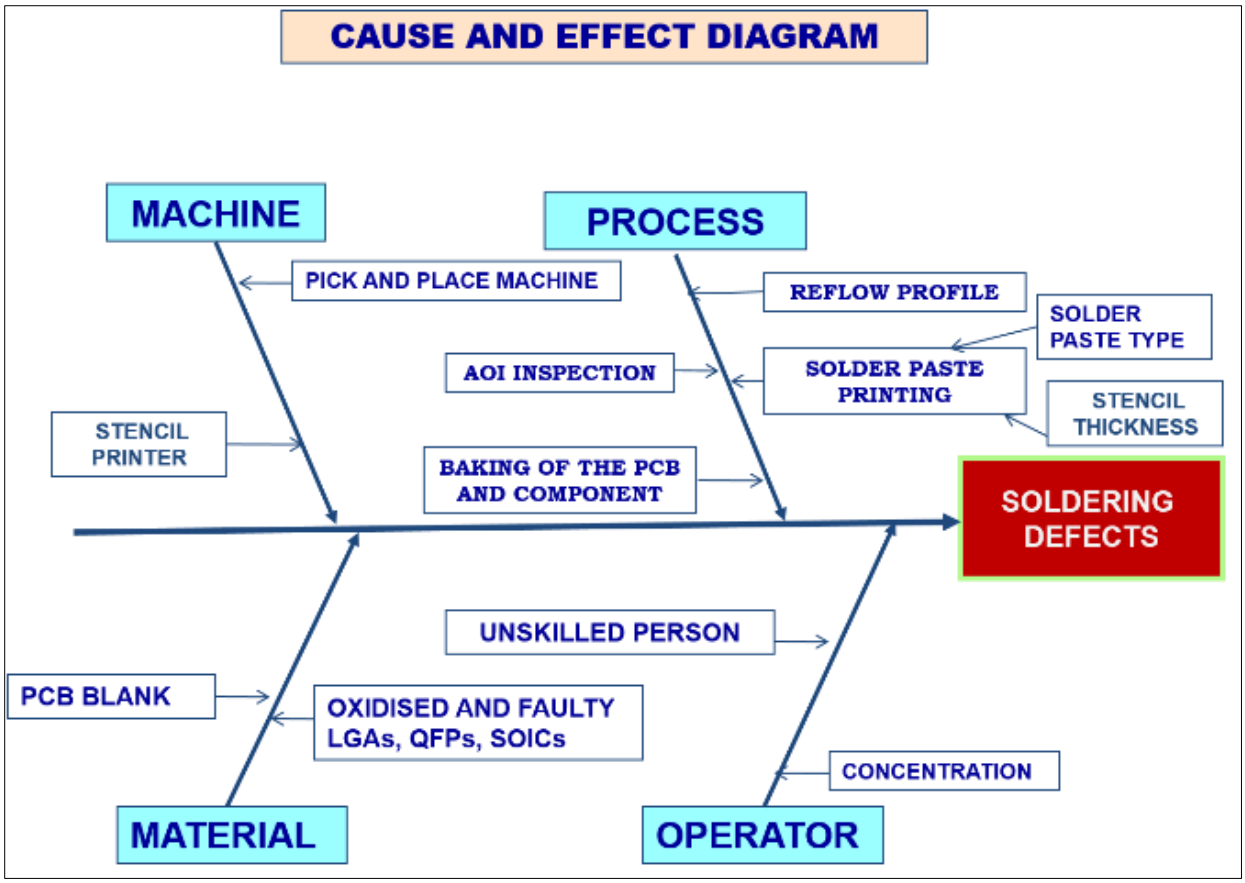


Figure 5 Cause and Effect diagram

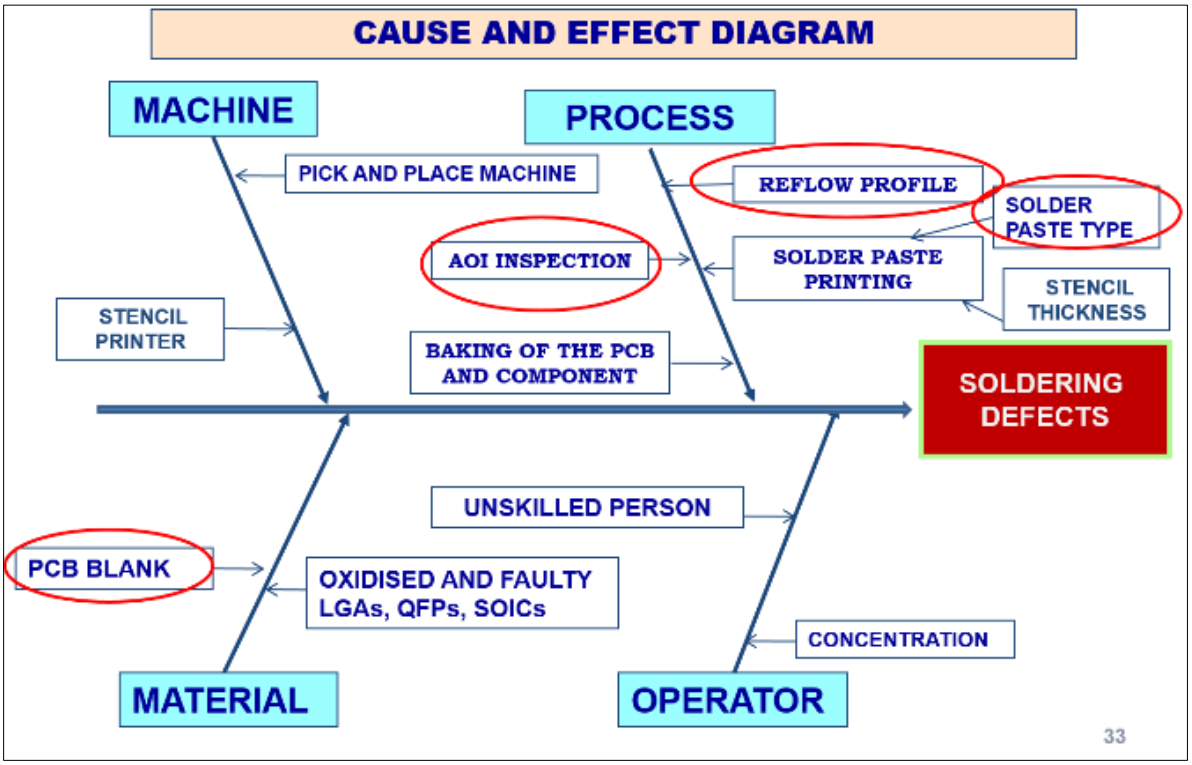


Figure 6 Problem identified areas

During analysis of the faults, following areas were identified to have potential faults in Figure 6.

3.1. Problem area

Defects occurred SMT process is shown in Figure 7. Where Tomb stone formation happened during reflow soldering[4][5].

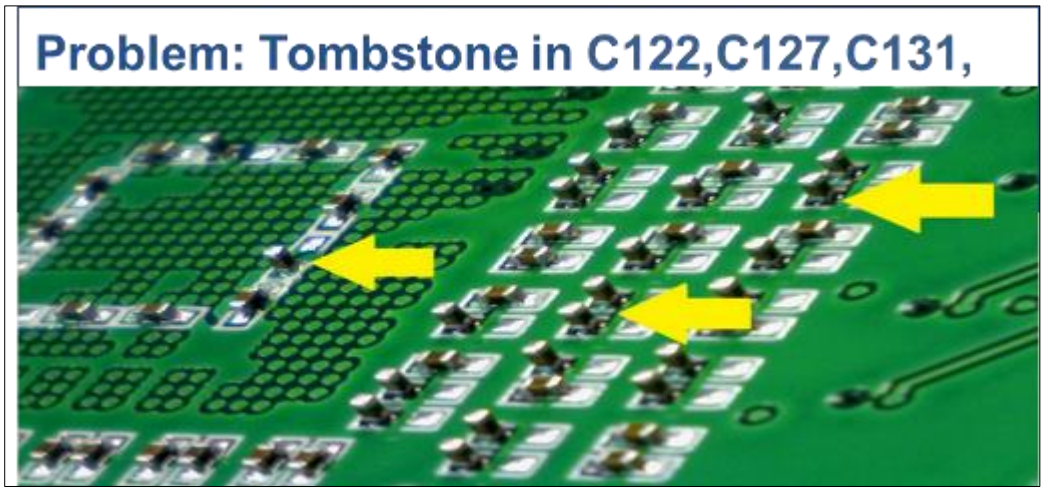


Figure 7 Tomb stone formation

The main cause for tombstone were as follows:

- Pad Design in PCB gerber was not as per IPC standard for 0201 chip components due to which unequal surface tension exists & lifts the component from one side causing tomb stoning defect or Manhattan defect [6].
- Type 4 solder paste is recommended for 0201 or smaller components for better solderability but used solder paste was type 3[7] [8].
  - In Reflow solder profile ramp up rate was little higher (>2 Degree/sec) causing the component to sudden exposure to temperature [9]. Due to this one side of the component has poor wettability causing unequal torque at one end and lifts the component.
  - Reflow time is <60secs causing poor solder ability [10].
  - AOI of all the PCBs was done on 2D AOI machine
  - In 2D AOI it was difficult to identify the Dry solder defect in 0201 chip components & lifted leads of ICs due to shadow effect [11].
- So most of the defects remain unidentified during inspection & PCBs offered to testing without touch up & rework.

4. Solution

After in-depth analysis of the problem, it was decided to have permanent solution of these problems.

It is resulted into changes in design of problematic areas. The design changes is shown in Table 1.

Table 1 Design Changes

Sl No.	Controllable Factors	Earlier Process	Improvement Plan
C1	Blank Pcb Design	Pad dimension for 0201 chip components in Gerber was not as per IPC standard.	Intimation will be given to Design Deptt. for change in Pad as per IPC standard
		Old stencil was as per previous gerber	New stencil will be made as new gerber.

4.1. Solder paste change

After in depth study of the solder paste, it was decided to change the solder paste since it suited for smaller size of components. Details is shown in Table 2.

Table 2 Solder Paste change

Sr No	Controllable Factor	Earlier Process	Improvement Plan
C2	Solder Paste Type.	Type 3 Solder Paste used.	Type 4 Solder Paste will be used for Pcb having 0201 or smaller chip components.
		Particle size in Type 3 Solder Paste was 25-45um.	Type 4 Solder pate will be used having particle size 20-38 um for good printability and wettability during reflow.

Table 3 Change in Reflow profiling

Sr No	Controllable Factor	Earlier Process	Improvement Plan
C3	Reflow Profile	In earlier reflow profile, there was high rising slope above TAL (Time above Liquidous) > 2 Degree per sec.	Type 4 Solder Paste will be used for Pcb having 0201 or smaller chip components.
		Reflow time was not in the range 60-90 secs as recommended in standard lead free profile.	Reflow profile will be done with reflow time 60-90 secs.

For better solderability, Reflow profile was analyzed and changed accordingly to suit for components. Detail is shown in Table 3.

Automated Optical Inspection was not able to detect soldering defects. After analysis it was found that AOI was done through 2D inspection system which was not capable enough to find tome stone defects. Later on it was decided to check through 3D inspection system. Detail is shown in Table 4.

Table 4 AOI Inspection methodology

Sr No	Controllable Factor	Earlier Process	Improvement Plan
C4	AOI Inspection.	Full lot was inspected through 2D AOI machine. Lots of defects were not noticed for small components 0201 size due to very small size and shadow effects.	1. Future lot will be inspected through 3D AOI for better defect identification. 2. After identification touch/rework will be done on defective pcbs. 3. After touch up again pcb will be inspected through 3D AOI system.

5. Results

After carrying out all modifications, once again pcbs were reflow soldered and then pcbs were subjected to functional test. It was found that after incorporation of changes, yield of pcb was better and result is shown in Figure 8.

Type of Fault	Tombstone	Dry Solder	Shorting (Bridging)	SHIFT	Billboard	Wrong Orientation	Missing Comp
No. of Defects	4	2	1	2	1	1	0
Defect detail	C119, C241, C258, C269	C173, C220	U25	C7, Y1	R328	U13	-

Defectives Vs Defects	
PCB tested	75
No. of Defectives Troubleshooted	11
No. of Defects in PCB's	11
Pending for troubleshooting	0
First Time Pass	64
FTP%	85.3%

Figure 8 Yeild of pcb after implementation

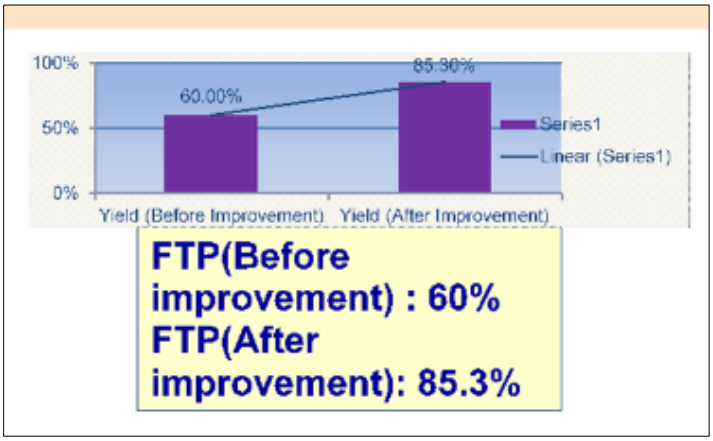
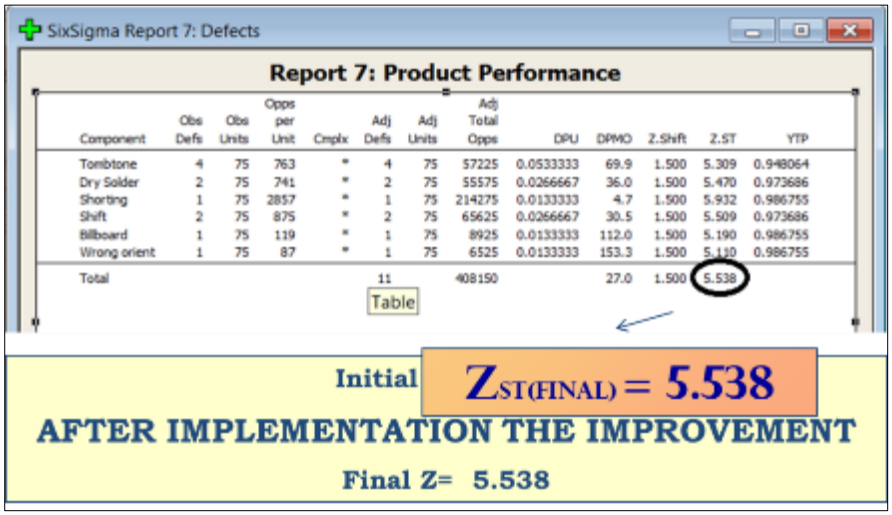


Figure 9 Yield of PCB

Yield of the Pcb before and after implementation is also shown in Figure 9.

Based on the result Z value is calculated for the process and shown in Figure 10.



Z value is increased from initial 4.475 to 5.538

Figure 10 Z- Value of the process

6. Conclusion

Process design is one of the important aspect of manufacturing process. Design of PCB should be done as per specification of the components and same way other process parameter values need to be arrived based on that and it will result to maximum yield of the product.

Other intangible benefits are

- Improved process
- Enhanced customer satisfaction
- Improvement in competency

Compliance with ethical standards

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Disclosure of conflict of interest

The authors declare no conflict of interests.

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