

World Journal of Advanced Engineering Technology and Sciences

eISSN: 2582-8266 Cross Ref DOI: 10.30574/wjaets Journal homepage: https://wjaets.com/



(RESEARCH ARTICLE)

Check for updates

Choosing optimal input and sampling frequencies for analog to digital converter testing

Francisco André Corrêa Alegria *

Instituto de Telecomunicações and Department of Electrotechnical Engineering and Computer Science, Technical Superior Institute, University of Lisbon, Av. Rovisco Pais, 1, Lisbon, Portugal.

World Journal of Advanced Engineering Technology and Sciences, 2023, 09(02), 124-134

Publication history: Received on 10 June 2023; revised on 18 July 2023; accepted on 20 July 2023

Article DOI: https://doi.org/10.30574/wjaets.2023.9.2.0215

Abstract

The main objective of this paper is to study of the ideal input and sampling frequencies, as well as determining the necessary number of samples for achieving coherent sampling. This aspect holds significant importance when it comes to testing analog-to-digital converters (ADCs) using various techniques such as the Histogram Test Method, Discrete Fourier Transform Method, or Sine-Fitting Method. The study conducted in this paper sheds light on a crucial consideration, which is the trade-off between testing duration and the proximity to the required frequencies. This trade-off is determined by the number of acquired samples. The balance between the amount of time spent on testing and the accuracy achieved in terms of the frequencies being targeted is of great importance. By exploring the ideal input and sampling frequencies, along with the determination of the necessary number of samples for coherent sampling, this research contributes to enhancing the understanding of ADC testing methodologies. It provides valuable information for researchers and practitioners in the field, enabling them to make informed decisions regarding the selection of appropriate testing techniques and algorithms based on their specific requirements and constraints. Ultimately, the findings presented in this paper have the potential to improve the efficiency and effectiveness of ADC testing processes, leading to more accurate and reliable results.

Keywords: Sampling; Analog-to-Digital Converter; Testing; Histogram Method; Signal Frequency

1. Introduction

Electrical signals play a crucial role in measurement and estimation applications across various fields. In information transmission, for example, electrical signals are used to convey information about physical quantities, such as voltage, current, temperature, pressure, and more. By measuring these signals, we can obtain valuable data that helps us understand and quantify the properties of the system or phenomenon being measured. Electrical signals can be precisely generated and manipulated, allowing for accurate measurement and estimation. The shape, frequency, and amplitude of electrical signals can be controlled and adjusted to optimize the measurement process, ensuring reliable and consistent results. Electrical signals can be processed and analyzed using various techniques to extract relevant information.

Signal processing methods, such as filtering, amplification, modulation, demodulation, and Fourier analysis, enable us to enhance the signal quality, remove noise, extract specific frequency components, and extract useful features for measurement and estimation purposes.

Many measurement applications rely on electrical sensors to convert physical quantities into electrical signals. Sensors like thermocouples, strain gauges, accelerometers, and pressure transducers generate electrical signals that are

^{*} Corresponding author: Alegria Francisco André Corrêa

Copyright © 2023 Author(s) retain the copyright of this article. This article is published under the terms of the Creative Commons Attribution Liscense 4.0.

proportional to the measured parameter. These signals can then be processed and analyzed to estimate the desired quantity accurately.

Electrical signals are used as reference standards for calibration purposes. Precisely known electrical signals, such as voltage or frequency standards, are employed to calibrate measurement instruments and ensure their accuracy. This calibration process establishes a traceable and reliable measurement system.

Electrical signals offer a non-intrusive method for measuring various parameters without physically interfering with the system under observation. For example, electrical signals can be used to measure electrical power consumption, vibration levels, or temperature without the need for direct contact or invasive techniques.

In applications such as industrial process control or medical monitoring, electrical signals enable real-time measurement and estimation, providing valuable feedback for immediate decision-making and control actions. Real-time monitoring and control systems rely on accurate and timely electrical signal measurements to ensure optimal performance and safety.

Choosing the appropriate signal frequency for stimulus signal in analog-to-digital converter (ADC) testing is important for several reasons. The Nyquist-Shannon sampling theorem emphasizes the need for a sampling frequency that is at least twice the maximum frequency component of the analog signal to prevent aliasing and ensure accurate reconstruction. By using different signal frequencies, the frequency response of the ADC can be characterized, revealing non-linearities, gain variations, and distortion across various frequency ranges.

Testing the dynamic range and linearity of the ADC requires selecting frequencies that challenge these aspects throughout the frequency spectrum. ADCs can introduce harmonic distortion and intermodulation distortion, which vary with frequency. Evaluating the ADC's noise performance and determining the signal-to-noise ratio necessitate choosing appropriate frequencies. Additionally, the choice of signal frequency helps prevent aliasing, where high-frequency components fold back into the ADC's frequency range. Thus, considering a range of frequencies enables a comprehensive assessment of the ADC's performance in terms of reconstruction, frequency response, dynamic range, distortion, noise, and aliasing prevention.

Different shapes of electrical signals are used in various applications depending on their specific characteristics and requirements. The sinusoidal waveform is one of the most common and fundamental waveforms in electrical engineering. It is characterized by a smooth, periodic oscillation that resembles a sine wave. Sinusoidal signals are widely used in applications such as power generation, audio systems, analog signal processing, and AC (alternating current) power transmission and ultrasonic ranging [1]. Triangular waveforms are characterized by a linear rise and fall with a sharp change in direction at the peaks and troughs. These waveforms are often used in applications such as motor control, modulation techniques, and audio synthesis. They can even be used for ADC testing [3-5]. Rectangular waveforms have equal positive and negative voltage durations with sharp transitions between the two levels. They are commonly used in digital electronics, pulse-width modulation (PWM) applications, clock signals, and data transmission. Sawtooth waveforms have a linear rise in voltage followed by a rapid drop back to the original level. They find applications in various areas such as music synthesis, sweep generators, and television raster scanning. Pulse waveforms have a distinct shape characterized by a narrow and brief period of high voltage (pulse) followed by a longer period of low voltage (rest). Pulse waveforms are used in applications such as pulse radar, timing circuits, pulse-width modulation, and digital communication. Exponential waveforms exhibit exponential growth or decay. They are used in applications such as charging and discharging of capacitors, exponential waveform generators, and time-domain reflectometry. Even constant signals have many applications like resistivity measurements [2].

The most popular techniques for testing an ADC [2, 6] involve sampling a sinusoidal input signal at a fixed rate (referred to as the sampling frequency, or fs), and then estimating various converter properties from the ADC output codes [7]. The Histogram Method is one of these techniques [8-15], which computes a histogram of the output codes to ascertain transition voltages and other parameters including gain, offset error, integral nonlinearity (INL), and differential nonlinearity (DNL). Another technique is called "sine-fitting," which uses least-squares estimation to fit a sinusoidal form to the ADC output codes [16-19]. The resulting error signal can be used to calculate aperture uncertainty, additive noise, and phase noise (jitter) [16, 20-23]. A discrete Fourier Transform is applied to the output in the case of the DFT test [7, 24-26]. The knowledge of the amount of additive noise or jitter [27, 30], for example, is paramount when computing the uncertainty of estimates obtained. Even a constant signal can be used to test an ADC in static conditions [31, 33].

To ensure that the amplitude distribution of the sampled voltages is clearly understood, all these testing techniques presuppose that the input signal is a perfect sinusoid that is sampled at particular time intervals. The signal needs to be captured for exactly one period of the stimulus signal to accomplish this. The stimulus signal frequency (f) must be substantially lower than the sampling frequency due to the enormous number of samples needed (sometimes millions) to assure good precision in the test findings, which is not ideal because the performance of ADCs depends on the input frequency. Time-equivalent sampling is frequently applied as a solution to this issue. To do this, samples must be collected throughout multiple sinusoid periods. It's crucial to make sure that the following relationship is verified [27]:

$$\rho = \frac{f}{f_s} = \frac{J}{M} \tag{1}$$

where *J* is the number of periods of the input signal during which the *M* samples are acquired. Fig.1 depicts the case where 40 samples are acquired during two periods of the stimulus signal.



Figure 1 Representation of 2 periods of a sinusoid during which 40 samples were acquired.

Because the integers 2 and 40 are not mutually prime (they have at least one common factor greater than 1, in this case the number 2), the number of distinct phases is just 20 as can be seen in Fig. 2.



Figure 2 Representation of the samples phases (*z*), normalized from 0 to *M*, for the case of 40 samples acquired during 2 sinusoid periods

Obtaining 39 samples in two separate time periods (as shown in Fig. 3) would result in 39 distinct sample phases. This is because the integers 2 and 39 are mutually prime, as illustrated in Fig. 4.



Figure 3 Representation of 2 periods of a sinusoid during which 39 samples were acquired.



Figure 4 Representation of the samples phases (*z*), normalized from 0 to *M*, for the case of 39 samples acquired during 2 sinusoid periods.

1.1. Frequency Errors

The distribution of sample phases might not be even because frequency errors can occur in both the sinewave and sampling generators. The number of samples must satisfy Eq. (2) in order to guarantee that an inaccuracy in the frequency ratio (Dr) results in an error in the distribution of phases of less than 50% of the ideal phase spacing.

$$\frac{\Delta\rho}{\rho} \le \frac{1}{2 \cdot J \cdot M} \tag{2}$$

This limit also guarantees that the variance of the number of counts of the cumulative histogram is lower than 1/4 [33-34].

Inserting (1) in (2) leads to

$$\Delta \rho \le \frac{1}{2M^2} \,, \tag{3}$$

where

$$\Delta \rho = \left| \rho_{ideal} - \rho \right|. \tag{4}$$

Again using (1) leads to

$$\Delta \rho = \left| \frac{f_{ideal}}{f_{s \ ideal}} - \frac{f}{f_s} \right|. \tag{5}$$

If we take into account the maximum relative errors of $\pm \epsilon$ and $\pm \delta$ in the real values of the frequency, Eq. (5) can be expressed as:

$$\Delta \rho = \left| \frac{f_{ideal}}{f_{s \ ideal}} - \frac{f_{ideal} \cdot (1 \pm \varepsilon_{f})}{f_{s \ ideal} \cdot (1 \pm \varepsilon_{f_{s}})} \right| =$$

$$= \frac{f_{ideal}}{f_{s \ ideal}} \left| 1 - \frac{1 \pm \varepsilon_{f}}{1 \pm \varepsilon_{f_{s}}} \right| = \frac{f_{ideal}}{f_{s \ ideal}} \left| \frac{\pm \varepsilon_{f_{s}} - (\pm \varepsilon_{f})}{1 \pm \varepsilon_{f_{s}}} \right|.$$
(6)

Expression (5) implies that

$$\frac{f_{ideal}}{f_{s ideal}} \left| \frac{\varepsilon_{f_s} - \varepsilon_f}{1 + \varepsilon_{f_s}} \right| \le \Delta \rho \le \frac{f_{ideal}}{f_{s ideal}} \left| \frac{\varepsilon_{f_s} + \varepsilon_f}{1 - \varepsilon_{f_s}} \right|.$$
(7)

If the value of the rightmost term is less than $\frac{1}{2M^2}$, then the value of $\Delta \rho$ will also be less than that value. Therefore, the number of samples must satisfy:

$$\frac{f_{ideal}}{f_{s\ ideal}} \left| \frac{\varepsilon_{f_s} + \varepsilon_f}{1 - \varepsilon_{f_s}} \right| \le \frac{1}{2M^2}.$$
(8)

As a result, an equation can be derived to determine the maximum number of samples that must be acquired consecutively:

$$M \le \sqrt{\frac{1}{2} \frac{f_{s \ ideal}}{f_{ideal}} \frac{\left|1 - \varepsilon_{f_s}\right|}{\varepsilon_{f_s} + \varepsilon_f}} = M_{\max}$$
(9)

1.2. Algorithms

It is not easy to choose an input frequency and sample count that satisfies both equations (1) and (9) at the same time. To solve this problem, different algorithms are examined in the part that follows.

1.3. Standard

The IEEE waveform digitizer standard [7] outlines an algorithm that relies on the observation that an integer and one of its multiples subtracted by 1 are mutually prime. The algorithm is presented as follows:

Find an integer, *n*, such that the desired frequency (f_d) is approximately f_s / n .

Let J = int(M / n) = the number of full cycles that can be recorder at this frequency.

Let $f = J \times f_s / (nJ - 1)$.

This guarantees *nJ*-1 distinct sample phases.

The first phase of the procedure described above involves choosing the value of the integer *n*, which stands for the number of samples collected during the course of one sinusoidal period. This is due to the fact that it is unclear whether the f_s/f_d ratio should be rounded up or down, as seen in

$$n = \left\lceil \frac{f_s}{f_d} \right\rceil \text{ or } n = \left\lfloor \frac{f_s}{f_d} \right\rfloor \text{ respectively}$$
(10)

For large values of M (>100), where and, Fig. 5 shows the actual frequency ratio f/f_s plotted against the planned frequency ratio f_d/f_s . Instances when the ratio f_s/f_d is rounded up or down are represented by the thin and thick lines, respectively. For instance, if the desired frequency is exactly half the sampling frequency ($\rho_d = 1/2$), there is no need for rounding ($n = f_s/f_d = 2$) because the ratio f_s/f_d is exactly two. This corresponds to the center of the picture, where each sinusoid period includes exactly 2 samples. Thus, the ratio f_s/f_d would be between 1 and 2 if the required frequency is greater than half the sampling frequency and less than the sampling frequency ($1/2 < \rho_d < 1$). If you rounded it up, you'd get two samples.



Figure 5 Representation of the relationship between the desired and actual frequency ratios. When f_s/f_d is rounded up, the thin line indicates that, and when it is rounded down, the thick line.

The value of *M* that should be used is not stated in the procedure suggested in [7]. One may presume that this value should be used to determine *J* if one were to refer to the preceding section, which says that the number of samples shouldn't be greater than M_{max} , which is given by (9). There is a drawback to this strategy, though. Although the algorithm makes sure that the number of samples to be obtained (*nJ*-1) is smaller than the amount chosen for *M*, this could lead to a frequency that is higher than desired, which would lower the bound M_{max} provided by (9) and result in a bigger number of samples (*nJ*-1) than M_{max} . Fig. 6 (thin line) shows this, where the relative difference between the actual number and



Figure 6 The intended frequency ratio is used to represent the relative difference of the number of samples as indicated by equation (11). When f_s/f_d is rounded up, the thin line indicates that, and when it is rounded down, the thick line. 25 ppm of frequency errors were employed.

(11)

This happens when the ratio f_s/f_d is rounded down to get *n*. Always rounding up f_s/f_d would be the appropriate strategy. By doing this, (9) will always be satisfied, as indicated by the thick line in Fig. 6. The thick line in Fig. 5 illustrates how this would likewise lead to a frequency lower than the desired one.

The actual frequency ratio and number of samples to acquire would be

$$\rho = \frac{J}{M} \text{ and } M = nJ - 1 \text{ with}$$

$$J = \left\lfloor \frac{M_{\text{max}}}{n} \right\rfloor \text{ and } n = \left\lceil \frac{f_s}{f_d} \right\rceil$$
(12)

1.4. Analytical

It should be noted that the maximum number of samples (M_{max}), which is specified by the frequency ratio (as stated in equation (9), is necessary for the frequency ratio to be calculated from equation (12). When M/J is used in place of f_{Sideal}/f_{ideal} in equation (9), the following two equations can be combined:

$$M \le \sqrt{\frac{1}{2} \frac{M}{J} \frac{\left|1 - \varepsilon_{f_s}\right|}{\varepsilon_{f_s} + \varepsilon_f}}$$
(13)

Using *M*=*nJ*-1, expression (13) can be rewritten as

$$M \leq \sqrt{\frac{1}{2} \frac{M}{\frac{M+1}{n}} \frac{\left|1-\varepsilon_{f_s}\right|}{\varepsilon_{f_s}+\varepsilon_f}}$$
(14)

After some simplification,

$$M(M+1) \le n \cdot \frac{1}{2} \frac{\left|1 - \varepsilon_{f_s}\right|}{\varepsilon_{f_s} + \varepsilon_f}$$
(15)

Solving the second order equation leads to

$$M \leq \frac{-1 + \sqrt{1 + 2n \frac{\left|1 - \varepsilon_{f_s}\right|}{\varepsilon_{f_s} + \varepsilon_f}}}{2}.$$
(16)

Inserting again *M*=*nJ*-1:

$$nJ - 1 \le \frac{1}{2} \left(-1 + \sqrt{1 + 2n \frac{\left|1 - \varepsilon_{f_s}\right|}{\varepsilon_{f_s} + \varepsilon_f}} \right).$$
(17)

And finally solving for J and rounding down the right member of (17) leads to

$$J = \left\lfloor \frac{1}{2n} \cdot \left(1 + \sqrt{1 + 2n \cdot \frac{\left| 1 - \varepsilon_{f_s} \right|}{\varepsilon_{f_s} + \varepsilon_f}} \right) \right\rfloor$$
(18)

The thick line in Fig. 7 demonstrates that, in comparison to the method described in, utilizing the expression derived in (13) is a more effective way to calculate *J* in terms of the number of samples (12).



Figure 7 Expression (18) is used to represent the relative difference between the number of samples defined by (11), as a function of the desired frequency ratio. The thick line shows the application of equation, whereas the thin line represents the best answer as indicated in III.C. (18). 25 ppm of frequency mistakes were employed.

The frequency however will still be in some cases far from the desired one (thick line in Fig. 8).



Figure 9 The actual frequency ratio is shown as a function of the desired one. When expression (18) is used, the situation is represented by the thick line, and when the best answer is employed (finding J that is mutually prime with M provided by (9)), the thin line is applied. 25 ppm of frequency errors were employed.

1.5. Optimal

We must make sure that *J* and *M* do not share any divisors. A computer can help with this since it is often used to process test data or execute the ADC test in the first place. Fig. 7 (thin line) and 8, in particular, which show that the actual frequency ratio is nearly similar to the targeted ratio, show the success of this strategy.

To achieve an optimal solution for sample acquisition in ADC testing, a recommended approach is to utilize the number of samples determined by equation (9):

$$M = \lfloor M_{\max} \rfloor \tag{19}$$

However, it is important to note that this value serves as an upper bound, and the objective is to search for an integer value, denoted as J, that is lower than the value

$$J_{\max} = \lfloor \rho_d \cdot M \rfloor \tag{20}$$

One crucial requirement in this process is to ensure that *J* and *M*, do not share any common divisors. This condition is necessary to maintain the integrity and accuracy of the sampling process. Since computing systems are commonly employed for processing test data or executing ADC tests, they can be leveraged to facilitate this search. The computational power and algorithms available in computers greatly aid in identifying suitable values for *J* and *M* that satisfy the non-divisor criterion.

The successful implementation of this strategy is evidenced by Fig. 7 and 8. Fig. 7, depicted by the thin line, illustrates that the actual frequency ratio achieved through this approach is remarkably close to the targeted ratio. This proximity signifies the effectiveness of the sampling methodology in accurately capturing the desired frequency range. Furthermore, Fig. 8 showcases the positive outcomes of the strategy, as the thin line demonstrates the maximum utilization of available samples.

By employing the optimal solution derived from equation (9), searching for a suitable *J* value, and ensuring the absence of common divisors between *J* and *M*, this approach offers a reliable and efficient method for sample acquisition in ADC testing. The reliance on computer-based processing facilitates the execution of this strategy and aids in achieving the desired frequency ratio with high fidelity. The presented figures provide visual evidence of the strategy's success, reinforcing its viability for accurate and precise ADC testing.

2. Conclusions

In the context of acquiring successive samples in ADC testing, there is a restriction on the maximum number of samples due to the need for evenly spaced phase samples, even in the presence of frequency errors. This constraint ensures that the acquired samples maintain a uniform distribution across the waveform, regardless of any frequency deviations.

To address this issue, the paper refers to a specific algorithm discussed in a prior work (reference [7]). The mentioned algorithm is further elucidated to provide a clearer understanding of its functioning. Additionally, the paper introduces equation (18) as a more practical approach to calculating the number of samples required for the given testing scenario. This equation offers a pragmatic method for determining the optimal number of samples needed for accurate sampling.

Moreover, the paper demonstrates the effectiveness of the suggested algorithm by showcasing the best approach. This approach involves conducting an exhaustive search for two mutually prime integers. Despite its increased computational complexity and the requirement for a computer-based implementation, this method offers distinct advantages. It allows for achieving proximity to the ideal input frequency, as indicated by the thin line in Fig. 7. Additionally, it maximizes the utilization of samples, as evidenced by the thin line in Figure 8. These outcomes highlight the superiority of the suggested approach in terms of capturing the desired frequency range with a higher degree of precision.

By presenting the algorithm in detail, introducing a practical calculation method, and showcasing the advantages of the best approach, the paper contributes to advancing the understanding of how to optimize sample acquisition in ADC testing. Researchers and practitioners can leverage this information to select appropriate techniques and algorithms that strike a balance between accuracy and efficiency in their specific testing scenarios. The findings highlight the potential for improved ADC testing methodologies that yield more reliable and precise results.

Compliance with ethical standards

Acknowledgments

This research was supported by Instituto de Telecomunicações and is funded by FCT/MCTES through national funds and when applicable co-funded EU funds under the project UIDB/EEA/50008/2020.

Disclosure of conflict of interest

No conflict of interest to disclosed.

References

- [1] Z. Dou, D. Karnaushenko, O. G. Schmidt and D. Karnaushenko, "A High Spatiotemporal Resolution Ultrasonic Ranging Technique With Multiplexing Capability," in IEEE Transactions on Instrumentation and Measurement, vol. 70, pp. 1-12, 2021, Art no. 6505012, doi: 10.1109/TIM.2021.3120129.
- [2] E. Martinho, F. Corrêa Alegria, A. Dionisio, C. Grangeia, F. Almeida, "3D-resistivity imaging and distribution of water soluble salts in Portuguese Renaissance stone bas-reliefs", Engineering Geology, Volumes 141–142, 2012, pp.33-44, ISSN 0013-7952, https://doi.org/10.1016/j.enggeo.2012.04.010.
- [3] A. Cruz Serra, F. Corrêa Alegria, R. Martins, M. da Silva, "Analog-to-digital Converter Testing—New Proposals", Computer Standards & Interfaces 26 (1), 3-13, 2004, doi:10.1016/S0920-5489(03)00057-6.
- [4] F. Corrêa Alegria, P. Arpaia, P. Daponte, A. Cruz Serra, "ADC histogram test using small amplitude input waves", XVI IMEKO World Congress 2000.
- [5] S. C. Vora and L. Satish, "ADC Static Characterization Using Nonlinear Ramp Signal," in IEEE Transactions on Instrumentation and Measurement, vol. 59, no. 8, pp. 2115-2122, August 2010, doi: 10.1109/TIM.2009.2031852.
- [6] F. Corrêa Alegria, P. Girão, V. Haasz, A. Cruz Serra, "Performance of Data Acquisition Systems from the User's Point of View", IEEE Transactions on Instrumentation and Measurement, vol. 53, nº 4, pp. 907-914, August 2004, doi: 10.1109/TIM.2004.830757.
- [7] IEEE, "IEEE Standard for digitizing waveform recorders IEEE Std 1057-1994", Institute of Eletrical and Electronics Engineers, Inc., SH94245, December 1994.
- [8] F. Corrêa Alegria, A. Cruz Serra, "Standard histogram test precision of ADC gain and offset error estimation", IEEE Transactions on Instrumentation and Measurement 56 (5), 1527-1531, 2007, doi: 10.1109/tim.2007.907978.
- [9] F. Corrêa Alegria, A. Moschitta, P. Carbone, A. Cruz Serra, D. Petri, "Effective ADC linearity testing using sinewaves", IEEE Transactions on Circuits and Systems I: Regular Papers 52 (7), 1267-1275, 2005, doi:10.1109/tcsi.2005.851393.
- [10] F. Corrêa Alegria, A. Cruz Serra, "Uncertainty in the ADC transition voltages determined with the histogram method" Proceedings of the 6th Workshop on ADC Modeling and Testing, Lisbon, 2001.
- [11] A. Cruz Serra, F. Corrêa Alegria, L. Michaeli, P. Michalko, J. Saliga, "Fast ADC testing by repetitive histogram analysis", 2006 IEEE Instrumentation and Measurement Technology Conference Proceedings, 2006, doi: 10.1109/imtc.2006.328161.
- [12] L. Michaeli, Fast dynamic methods of the systematic error autocorrection, in: Proceedings of 5th IMEKO TC-4 International Symposium, Vienna, April 1992, 1992, pp. 247 249.
- [13] V. Pálfi, "An Improved Sine Wave Histogram Test Method for ADC Characterization," in IEEE Transactions on Instrumentation and Measurement, vol. 68, no. 10, pp. 3446-3455, Oct. 2019, doi: 10.1109/TIM.2018.2878593.
- [14] K. Y. Tan, J. Q. Q. Cheng and J. H. Chuah, "Investigation of Static Analog-to-Digital Converter Nonlinearity Measurement Using Histogram and Servo-Loop Method," 2018 IEEE 5th International Conference on Smart Instrumentation, Measurement and Application (ICSIMA), Songkhla, Thailand, 2018, pp. 1-4, doi: 10.1109/ICSIMA.2018.8688768.
- [15] T. Moosazadeh and M. Yavari, "A Calibration Technique for Pipelined ADCs Using Self-Measurement and Histogram-Based Test Methods," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, no. 9, pp. 826-830, Sept. 2015, doi: 10.1109/TCSII.2015.2435851.
- [16] F. Corrêa Alegria, A. Cruz Serra, "Gaussian jitter-induced bias of sine wave amplitude estimation using threeparameter sine fitting", IEEE Transactions on Instrumentation and Measurement 59 (9), 2328-2333, 2009, doi: 10.1109/tim.2009.2034576.
- [17] F. Corrêa Alegria, A. Cruz Serra, "Uncertainty of the estimates of sine wave fitting of digital data in the presence of additive noise", 2006 IEEE Instrumentation and Measurement Technology Conference Proceedings, 2006.
- [18] D. Belega and D. Petri, "Statistical Performance of the Effective-Number-of-Bit Estimators Provided by the Sine-Fitting Algorithms," in IEEE Transactions on Instrumentation and Measurement, vol. 62, no. 3, pp. 633-640, March 2013, doi: 10.1109/TIM.2012.2218679.
- [19] B. Renczes, I. Kollár and T. Dabóczi, "Efficient Implementation of Least Squares Sine Fitting Algorithms," in IEEE Transactions on Instrumentation and Measurement, vol. 65, no. 12, pp. 2717-2724, December 2016, doi: 10.1109/TIM.2016.2600998.

- [20] M. Emmenegger, F. Jenni, R. Kunzi, H. Jaeckle and S. Schnabel, "Analysis and calibration of a high precision AD converter," 2007 European Conference on Power Electronics and Applications, Aalborg, Denmark, 2007, pp. 1-10, doi: 10.1109/EPE.2007.4417276.
- [21] L. Xu and D. Chen, "A low-cost jitter estimation and ADC spectral testing method," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, Portugal, 2015, pp. 2277-2280, doi: 10.1109/ISCAS.2015.7169137.
- [22] V. Pálfi and I. Kollár, "Efficient execution of ADC test with sine fitting with verification of excitation signal parameter settings," 2012 IEEE International Instrumentation and Measurement Technology Conference Proceedings, Graz, Austria, 2012, pp. 2662-2667, doi: 10.1109/I2MTC.2012.6229502.
- [23] D. Belega and D. Petri, "Analog-to-Digital Converter Dynamic Testing by Linearized Four-Parameter Sine-Fit Algorithm," 2021 IEEE 6th International Forum on Research and Technology for Society and Industry (RTSI), Naples, Italy, 2021, pp. 502 506, doi: 10.1109/RTSI50628.2021.9597328.
- [24] "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," in IEEE Std 1241-2010 (Revision of IEEE Std 1241-2000), vol., no., pp.1-139, 14 Jan. 2011, doi: 10.1109/IEEESTD.2011.5692956.
- [25] D. Agrez, "Analysis of the Residual Spectrum in ADC Dynamic Testing," in IEEE Transactions on Instrumentation and Measurement, vol. 58, no. 3, pp. 506-511, March 2009, doi: 10.1109/TIM.2009.2005558.
- [26] P. Carbone, E. Nunzi and D. Petri, "Windows for ADC dynamic testing via frequency-domain analysis," in IEEE Transactions on Instrumentation and Measurement, vol. 50, no. 6, pp. 1571-1576, Dec. 2001, doi: 10.1109/19.982947.
- [27] J. Blair, "Histogram measurement of ADC nonlinearities using sine waves", IEEE Trans. on Instrumentation and Measurement, vol. 43, nº 3, pp. 373-383, June 1994, doi: 10.1109/19.293454.
- [28] F. Corrêa Alegria, A. Cruz Serra, "Uncertainty of ADC random noise estimates obtained with the IEEE 1057 standard test", IEEE transactions on instrumentation and measurement 54 (1), pp. 110-116, January 2005.
- [29] F. Corrêa Alegria, P. Girão, V. Haasz, A. Cruz Serra, "Performance of Data Acquisition Systems from the User's Point of View", 20th IEEE Instrumentation and Measurement Technology Conference, pp. 940-945, May, 2003, doi: 10.1109/imtc.2003.1207891.
- [30] S. Shariat-Panahi, F. Corrêa Alegria, A. Mànuel, A. Cruz Serra, "IEEE 1057 jitter test of waveform recorders", IEEE Transactions on Instrumentation and Measurement 58 (7), 2234-2244, 2009, doi: 10.1109/tim.2009.2013674.
- [31] A. J. Ginés, E. J. Peralías and A. Rueda, "An adaptive BIST for INL estimation of ADCs without histogram evaluation," 2010 IEEE 16th International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW), La Grande Motte, France, 2010, pp. 1-6, doi: 10.1109/IMS3TW.2010.5502997.
- [32] S. C. Vora and L. Satish, "ADC Static Nonlinearity Estimation Using Linearity Property of Sinewave," in IEEE Transactions on Instrumentation and Measurement, vol. 60, no. 4, pp. 1283-1290, April 2011, doi: 10.1109/TIM.2010.2084773.
- [33] P. Carbone, G. Chiorboli, "ADC sinewave histogram testing with quasi-coherent sampling", Proceedings of the 17th IEEE Instrumentation and Measurement Technology Conference, Baltimore, MD, USA, vol. 1, pp. 108-113, May 1-4, 2000, doi: 10.1109/imtc.2000.846837.
- [34] F. Corrêa Alegria, A. Cruz Serra, "Influence of Frequency Errors in the Variance of the Cumulative Histogram", Conference on Precision Electromagnetic Measurements, pp. 585-586, May 2000, doi: 10.1109/cpem.2000.851145.

Authors short biography

Francisco ALEGRIA was born in Lisbon, Portugal, on July 2, 1972. He received the Diploma, M.S., and Ph.D. degrees in electrical engineering and computers from the Instituto Superior Técnico (IST), University of Lisbon, Portugal, in 1995, 1997, and 2002, respectively. He has been a member of the teaching and research staff of IST since 1997. His current research interests include ADC characterization techniques, automatic measurement systems, sensors and actuators.