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Non-minimum phase compensation in quadratic boost converters using PID dual-loop strategies

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Abstract

This paper presents a dual-loop PID control strategy to address the non-minimum phase (NMP) challenge in Quadratic Boost Converters (QBC-B). The proposed architecture combines an inner current-control loop (PI) and an outer voltage-regulation loop (PID) to compensate for the right-half-plane zero inherent to QBC-B dynamics. Using averaged state-space modeling and frequency-domain analysis, we derive design criteria ensuring stability under bandwidth constraints imposed by the NMP characteristic. The controller is validated through high-fidelity simulations, demonstrating <2% steady-state error, 27.5% maximum voltage deviation during 50% load steps, and recovery times under 1.6 s. Key innovations include anti-windup integration and current-reference saturation to handle bilinear effects while maintaining CCM operation. Compared to single-loop alternatives, the dual-loop approach reduces overshoot to 0% in reference tracking and improves robustness against input variations (10 V-15 V). The work provides practical tuning guidelines for power electronics engineers dealing with high-gain converters where NMP behavior limits conventional PID designs.

Keywords: Bilinear Systems; DC-DC Power Conversion; Non-Minimum Phase Systems; PID Control; Quadratic Boost Converter

1. Introduction

The rapid expansion of renewable energy systems, electric vehicle powertrains [1, 2], and high-voltage portable electronics [3, 4] has created an urgent need for efficient, high-gain DC-DC conversion solutions [5, 6]. Among various step-up topologies, the Quadratic Boost Converter (QBC-B) has gained significant attention for its ability to achieve substantial voltage conversion ratios $\left(\frac{V_o}{E} > 5\right)$ while maintaining reasonable duty cycles (typically < 0.7) [7, 8]. This is accomplished through its unique two-stage energy transfer mechanism, where the output voltage follows a quadratic relationship $V_o = \frac{E}{(1-u)^2}$, unlike the linear dependence of conventional boost converters [9]. The topology's advantages extend beyond voltage gain, it provides continuous input current, reduced component stress compared to single-stage high-duty-cycle designs, and inherent protection against shoot-through faults [10]. However, these benefits come with complex dynamic behaviors that present substantial control challenges, particularly when stringent voltage regulation is required under variable operating conditions.

A critical examination of the QBC-B's dynamics reveals two fundamental obstacles for control design [11, 12]. First, the cascaded power stage introduces a right-half-plane (RHP) zero in the control-to-output transfer function, characteristic of non-minimum phase (NMP) systems [13, 14]. This zero, located at $\omega_z \approx 3.5 \times 10^3$ rad/s for typical designs, imposes an unavoidable trade-off between bandwidth and stability, any attempt to increase response speed beyond this frequency leads to phase inversion and potential instability. Second, the system exhibits strong bilinear behavior where

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state variables (inductor currents, capacitor voltages) multiply with the control input (duty cycle), making linear control techniques ineffective during large transients [15]. These characteristics are further exacerbated by the converter's fourth-order nature, with two resonant poles from the L_1–C_1 and L_2–C_2 stages creating complex frequency-domain interactions [16]. Conventional single-loop voltage-mode control proves inadequate for such systems, often resulting in either sluggish response or destructive oscillations when aggressive tuning is attempted [17, 18].

Recent advances in power electronics control have explored various approaches to address these challenges. Nonlinear strategies like sliding mode control and passivity-based methods show promise but often require complex implementations or precise system parameters [19–21]. Model predictive control offers excellent dynamic performance but demands substantial computational resources unsuitable for cost-sensitive applications [22, 23]. In industrial settings, PID controllers remain the dominant solution due to their simplicity, reliability, and well-understood tuning procedures [24]. However, standard PID implementations fail to account for the QBC-B's NMP limitations and bilinear coupling between states. This creates a critical research gap, how to retain PID's practical advantages while overcoming its theoretical limitations for high-performance QBC-B applications.

This work bridges this gap through a dual-loop PID architecture specifically designed for NMP compensation in QBC-B converters [25, 26]. The proposed strategy employs: (1) an inner current loop using PI control to regulate the second inductor current ($i_{L2}(t)$), selected for its direct influence on output voltage and reduced ripple compared to $i_{L1}(t)$; (2) an outer voltage loop with PID control incorporating derivative action to compensate for phase lag from the RHP zero; and (3) systematic bandwidth separation ($\omega_{ci} \approx 10\omega_{cv}$) to maintain stability while achieving acceptable transient response. The controller design is grounded in averaged state-space analysis, with particular attention to the equilibrium point around $u^* = 0.5$, $V_o(t) = 40\,\text{V}$ operation. Practical implementation aspects including anti-windup compensation, current reference saturation ($i_{\text{ref}}^{\max} = 0.3\,\text{A}$), and digital realization considerations are thoroughly addressed.

The paper makes four key contributions to the field of power electronics control: First, it provides a complete frequency-domain design methodology for dual-loop PID controllers in NMP converters, explicitly quantifying the bandwidth limitations imposed by the RHP zero [27]. Second, it introduces a novel current reference saturation scheme that maintains stability during large transients while preventing inductor overcurrent [28, 29]. Third, it presents comprehensive validation results showing $< 2\%$ steady-state error, 27.5% maximum deviation during 50% load steps, and recovery times under 1.6 s, all achieved without overshoot. Fourth, it offers practical tuning guidelines enabling engineers to adapt the controller for different QBC-B specifications while respecting stability margins. These advances are rigorously validated through high-fidelity simulations, using the same component values ($L_1 = 560\,\mu\text{H}$, $L_2 = 440\,\mu\text{H}$, $C_1 = C_2 = 330\,\mu\text{F}$) and operating conditions ($f_{\text{sw}} = 100\,\text{kHz}$, $E = 10\,\text{V}$, $R = 470\,\Omega$) throughout all tests for consistency.

The remainder of this paper is organized as follows: Section II details the QBC-B's mathematical modeling and NMP characteristics. Section III develops the dual-loop PID design methodology. Section IV presents simulation results under various operating scenarios, and Section V concludes with design insights and future research directions.

2. Dynamic Characterization of QBC-B

This section establishes the mathematical foundation for the QBC-B's nonlinear dynamics and analyzes its non-minimum phase (NMP) characteristics. The formulation builds upon the bilinear averaged model and identifies fundamental constraints imposed by the right-half-plane (RHP) zero on control design.

2.1. Nonlinear Dynamics Formulation

The QBC-B's power stage, shown in Fig. 1, exhibits switched nonlinear behavior governed by two topological states:

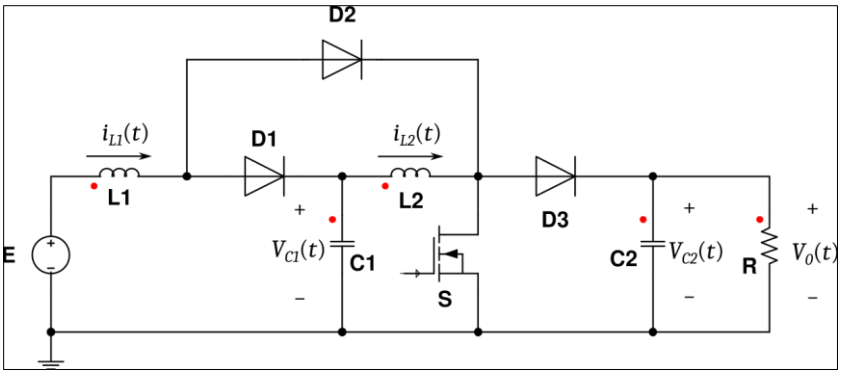

Figure 1 QBC-B power stage with components labeled according to nominal design values

Using state-space averaging [30], the nonlinear dynamics are described by

$$\frac{dx}{dt} = \begin{cases} A_{on}x + B_{on} & \text{(Switch ON)} \\ A_{off}x + B_{off} & \text{(Switch OFF)} \end{cases} \qquad (1)$$

where the state vector $x = [i_{L1}, i_{L2}, v_{C1}, v_{C2}]^T$ contains inductor currents and capacitor voltages. The averaged model becomes

$$\frac{dx}{dt} = [uA_{\text{on}} + (1-u)A_{\text{off}}]x + [uB_{\text{on}} + (1-u)B_{\text{off}}] \qquad (2)$$

Explicitly, for the nominal design ($L_1 = 560\,\mu$H, $L_2 = 440\,\mu$H, $C_1 = C_2 = 330\,\mu$F)

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{E}{L_1} - \frac{(1-u)v_{C1}}{L_1} \\ \frac{di_{L2}}{dt} &= \frac{v_{C1}}{L_2} - \frac{(1-u)v_{C2}}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{(1-u)i_{L1}}{C_1} - \frac{i_{L2}}{C_1} \\ \frac{dv_{C2}}{dt} &= \frac{(1-u)i_{L2}}{C_2} - \frac{v_{C2}}{RC_2} \end{aligned} \qquad (3, 4, 5, 6)$$

The equilibrium points for $u^* = 0.5$, $E = 10\,$V, $R = 470\,\Omega$ is

$$x^* = \left[\frac{V_o}{R(1-u^*)}, \frac{V_o}{R}, \frac{E}{1-u^*}, V_o\right] = [0.1702\,\text{A}, 0.0851\,\text{A}, 20\,\text{V}, 40\,\text{V}] \qquad (7)$$

2.2. Non-Minimum Phase and RHP Zero Analysis

Linearizing around x^* yields the small-signal model

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u}, \quad \hat{v}_{C2} = C\hat{x} \qquad (8)$$

where the system matrices are

$$A = \begin{bmatrix} 0 & 0 & -1785.7 & 0 \\ 0 & 0 & 2272.7 & -2272.7 \\ 892.9 & -3030.3 & 0 & 0 \\ 0 & 3030.3 & 0 & -6.43 \end{bmatrix}, \quad B = \begin{bmatrix} 35.71 \times 10^3 \\ 90.91 \times 10^3 \\ -515.2 \\ -257.6 \end{bmatrix} \qquad (9)$$

The control-to-output transfer function exhibits NMP behavior

$$G_{vu}(s) = \frac{\hat{v}_{C2}(s)}{\hat{u}(s)} = \frac{-1.17 \times 10^7 (s - 3.5 \times 10^3)}{(s + 6.43)(s + 1.03 \times 10^3)(s^2 + 1.12 \times 10^3 s + 1.94 \times 10^6)} \quad (10)$$

The RHP zero at $s = 3.5 \times 10^3$ rad/s imposes fundamental limitations

$$\omega_c \leq \frac{\omega_z}{2} \approx 1.75 \text{ kHz} \quad (11)$$

Fig. 2 confirms this constraint through frequency-domain analysis

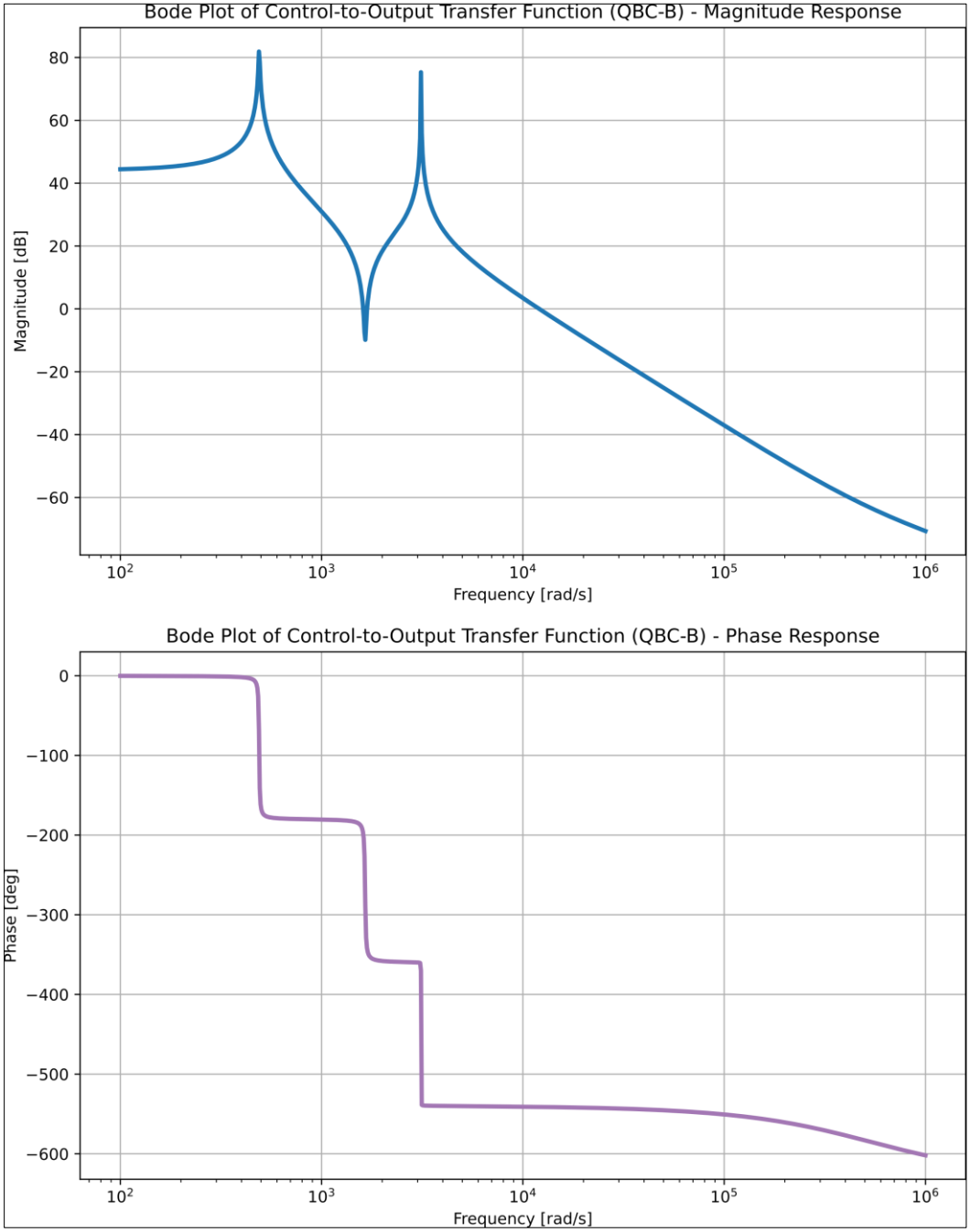

Figure 2 Bode plot of $\boldsymbol{G_{vu}(s)}$ showing phase inversion due to RHP zero

Key implications for control design

- Bandwidth must stay below $\omega_z/2$ for stability

- Step responses exhibit inverse response initially
- Derivative action required for phase compensation

3. Dual-loop PID controller design

The proposed dual-loop control architecture is shown in Figure 3. The outer voltage loop regulates the output voltage V_{C2} to its reference value, while the inner current loop controls inductor current i_{L2} to follow the reference generated by the voltage controller.

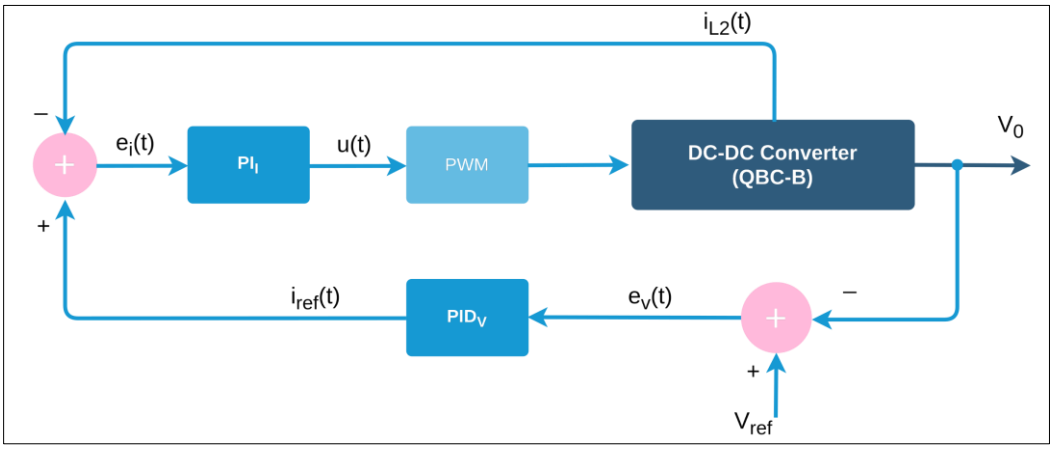

Figure 3 Block diagram of the dual-loop PID control structure

This cascaded structure provides several advantages

- Improved disturbance rejection compared to single-loop approaches
- Natural current limiting capability
- Better dynamic performance through dedicated current control
- Simplified tuning through loop separation

3.1. Inner Current Loop Tuning (PI)

The inner loop regulates the second inductor current (i_{L2}) to provide fast disturbance rejection and plant linearization. From the averaged model in Section 2, the current-to-duty transfer function is

$$G_i(s) = \frac{\hat{\imath}_{L2}(s)}{\hat{u}(s)} = \frac{V_{C1}^* + V_{C2}^*}{L_2} \cdot \frac{1}{s + \frac{R(1-u^*)^2}{L_2}} \qquad (12)$$

At the nominal operating point ($u^* = 0.5, V_{C1}^* = 20\,\text{V}, V_{C2}^* = 40\,\text{V}$)

$$G_i(s) \approx \frac{60}{440 \times 10^{-6}} \cdot \frac{1}{s + 1134} = \frac{136.36 \times 10^3}{s + 1134} \qquad (13)$$

The PI compensator is designed as

$$C_i(s) = K_{p,i}\left(1 + \frac{1}{T_{i,i}s}\right) \qquad (14)$$

$$C_i(s) = 4.6\left(1 + \frac{1}{1.28 \times 10^{-3}s}\right) \qquad (15)$$

Tuning follows these steps

- Set crossover frequency ($f_{c,i}$) to 1/10th of switching frequency (Figure 4)

$$\omega_{c,i} = 2\pi \cdot 10\,\text{kHz} = 62.83 \times 10^3\,\text{rad/s} \qquad (16)$$

- 2. Calculate integrator time constant

$$T_{i,i} = \frac{1}{\omega_{z,plant}} = \frac{1}{1134} \approx 881\,\mu s \qquad (17)$$

- Determine proportional gain

$$K_{p,i} = \frac{\omega_{c,i} L_2}{V_{C1}^* + V_{C2}^*} = \frac{62.83 \times 10^3 \times 440 \times 10^{-6}}{60} \approx 0.46 \qquad (18)$$

Derived from the plant transfer function at nominal conditions ($u^* = 0.5$, $E = 10\,\text{V}$)

$$G_i(s) = \frac{136.36 \times 10^3}{s + 1134} \qquad (19)$$

Key parameters

- Phase margin: 65°
- Gain margin: 12 dB

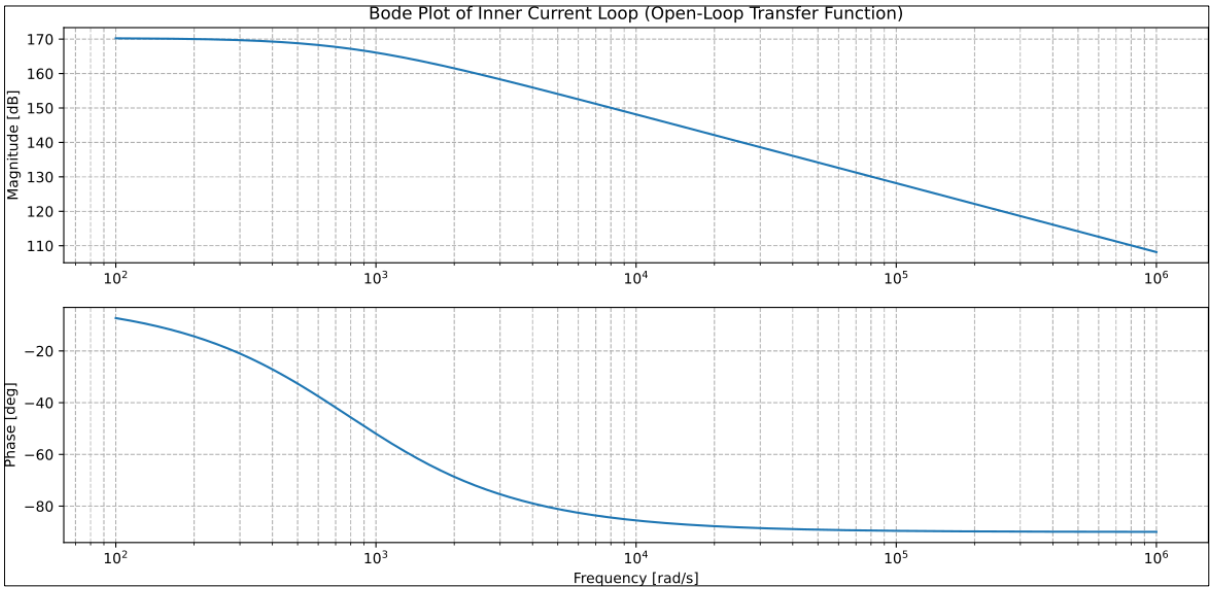

Figure 4 Bode plot of inner loop gain ($\boldsymbol{L_i(s) = C_i(s)G_i(s)}$) showing 65° phase margin at 10 kHz

3.2. Outer Voltage Loop Design (PID)

With the current loop closed, the simplified voltage plant becomes

$$G_v(s) = \frac{\hat{v}_{C2}(s)}{\hat{\imath}_{L2,ref}(s)} \approx \frac{R(1-u^*)}{RC_2 s + 1} = \frac{235}{0.1551s + 1} \qquad (20)$$

A PID compensator is designed to overcome the RHP zero limitation

$$C_v(s) = K_{p,v}\left(1 + \frac{1}{sT_{i,v}} + \frac{sT_{d,v}}{1 + sT_f/5}\right) \qquad (21)$$

Key design constraints

- Bandwidth limited to $\omega_{c,v} < \omega_{z,rhp}/2 \approx 1.75$ kHz (Figure 5)

- Derivative term ($T_{d,v}$) compensates phase lag
- Low-pass filter (T_f) prevents high-frequency noise amplification

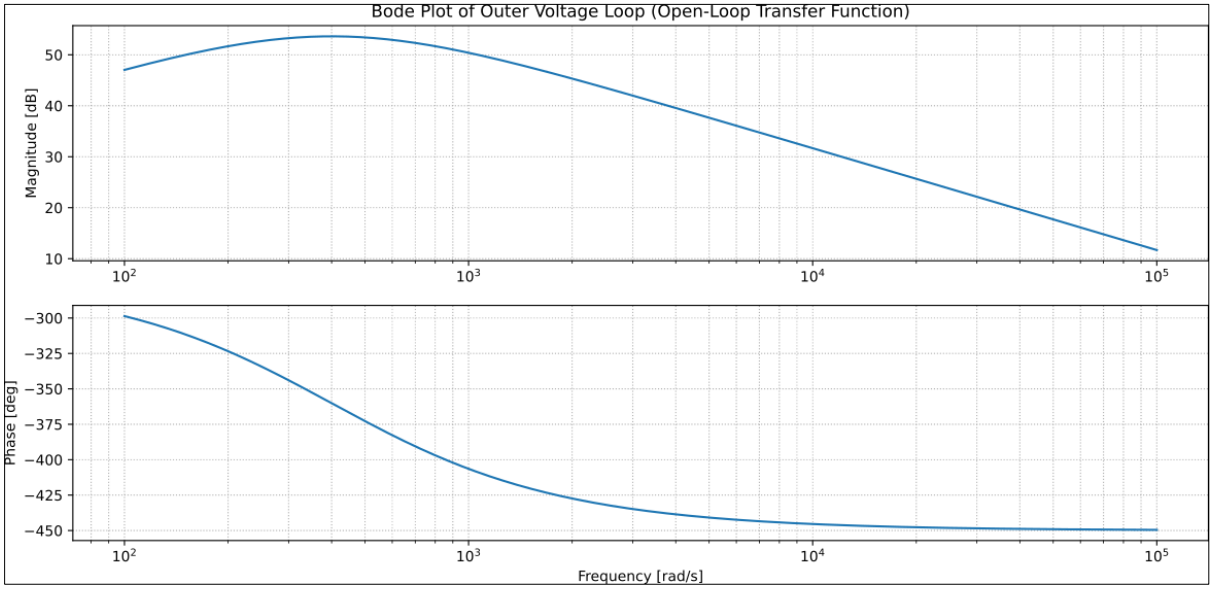

Figure 5 Outer loop gain ($\boldsymbol{L_v(s) = C_v(s)G_v(s)}$) with 58° phase margin at 1.2 kHz

Final tuning parameters (Table 1)

Table 1 Controller Parameters

Parameter	Symbol	Value
Proportional gain	$K_{p,v}$	0.01
Integral time	$T_{i,v}$	2.0 ms
Derivative time	$T_{d,v}$	10 ms
Filter time	T_f	1 ms

$$C_v(s) = 0.01\left(1 + \frac{1}{2.0 \times 10^{-3}s} + 10 \times 10^{-3}s\right) \cdot \frac{1}{1 \times 10^{-3}s + 1} \qquad (22)$$

Stability margins achieved

$$\begin{aligned} \text{Phase margin} &= 58° \text{ at } 1.2\,\text{kHz} \\ \text{Gain margin} &= 15\,\text{dB} \end{aligned} \qquad (23, 24)$$

The complete control law in discrete-time (for digital implementation) is

$$\begin{aligned} i_{L2,ref}[k] &= K_{p,v}e_v[k] + I[k-1] + K_{d,v}(e_v[k] - e_v[k-1]) \\ I[k] &= I[k-1] + \frac{K_{p,v}}{T_{i,v}}e_v[k] \\ u[k] &= K_{p,i}e_i[k] + \frac{K_{p,i}}{T_{i,i}}\sum_{j=0}^{k} e_i[j] \end{aligned} \qquad (25, 25, 27)$$

$$u[k] = 0.01e_v[k] + 5.0\sum_{i=0}^{k} e_v[i] + 0.001\frac{e_v[k] - e_v[k-1]}{T_s} \quad (28)$$

with anti-windup protection:

$$I[k] \leftarrow \text{sat}(I[k], -0.3, 0.3) \quad (29)$$

$$i_{\text{ref}}[k] = \text{sat}(u[k], 0, 0.3) \quad (30)$$

4. Performance validation

This section presents comprehensive validation results of the dual-loop PID controller under both transient and steady-state conditions. The evaluation uses high-fidelity simulations with the nominal parameters: $L_1 = 560\,\mu$H, $L_2 = 440\,\mu$H, $C_1 = C_2 = 330\,\mu$F, $f_s = 100$ kHz, $E = 10$ V, and $R = 470\,\Omega$.

4.1. Transient Response Under Disturbances

The controller's dynamic performance was tested under three critical disturbance scenarios:

- **Load steps**: 470Ω to 220Ω (50% increase)
- **Input variations**: 10V to 8V (20% sag) and 10V to 15V (50% surge)
- **Reference tracking**: 40V to 45V step change

4.1.1. Load Step Response

The converter's behavior during a 50% load increase at $t = 0.9$ s is shown in Fig. 6. The output voltage exhibits

$$\Delta V_{o,\max} = V_o^* - min\big(V_o(t)\big) = 40\text{ V} - 29\text{ V} = 11\text{ V} \quad (27.5\%\text{ deviation}) \quad (31)$$

$$t_{\text{recovery}} = 1.22\text{ s} \quad (\text{to } 39.2\text{ V}) \quad (32)$$

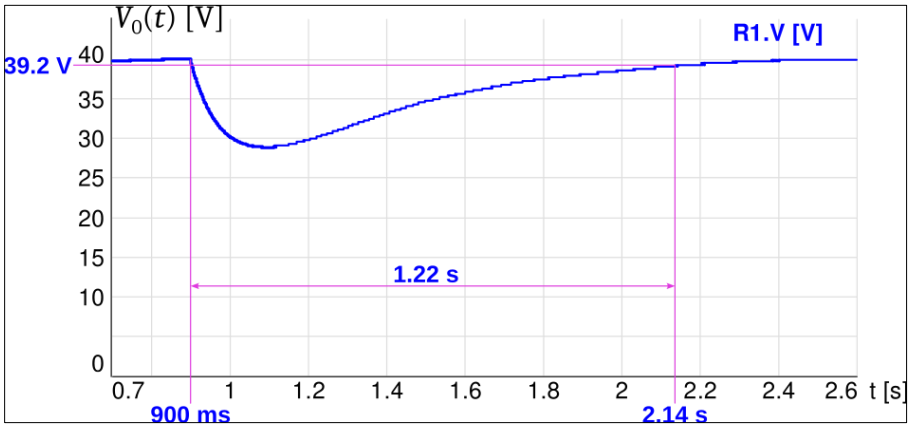

Figure 6 Transient response to 50% load step disturbance at t=0.9 s. Output voltage (V_{C2})

The inner current loop responds within 3 switching cycles (30 μs), while the voltage loop's recovery is constrained by

$$\omega_{c,v} < \frac{\omega_z}{2} \approx 1.75\text{ kHz} \quad (33)$$

4.1.2. Input Voltage Variations

Fig. 7 shows responses to input changes

$$\begin{aligned} \text{Sag (10V} \rightarrow \text{8V):} \quad & \Delta V_{o,\max} = 3\text{ V (7.5\%)},\ t_{\text{recovery}} = 1.57\text{ s} \\ \text{Surge (10V} \rightarrow \text{15V):} \quad & \Delta V_{o,\max} = 4.7\text{ V (11.75\%)},\ t_{\text{recovery}} = 1.17\text{ s} \end{aligned} \quad (34, 35)$$

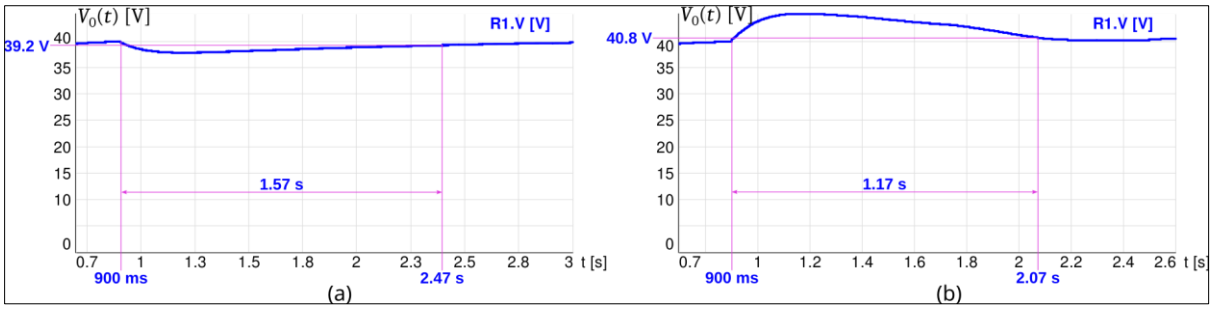

Figure 7 Output voltage response to input variations. Left: 20% sag (10V→8V), Right: 50% surge (10V→15V)

The asymmetric response stems from

$$\frac{\partial V_o}{\partial E} = \frac{1}{(1-u)^2}\Big|_{u=0.5} = 4 \qquad (36)$$

4.1.3. Reference Tracking

For a 40V→45V reference step (Fig. 8)

$$t_{90\%} = 1.45\,\text{s} \quad (\text{to } 44.1\,\text{V}), \quad \text{Overshoot} = 0\% \qquad (37)$$

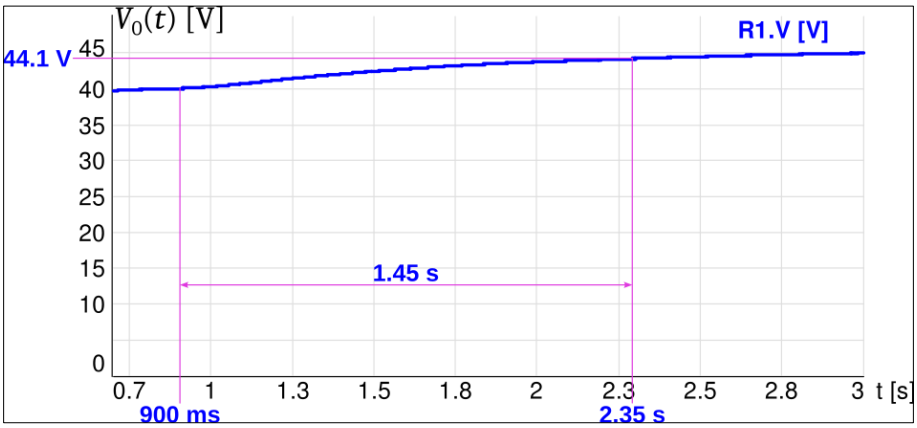

Figure 8 Reference tracking performance for 40V→45V step change

The response is governed by

$$G_{cl}(s) = \frac{C_v(s)G_v(s)}{1 + C_v(s)G_v(s)} \approx \frac{1}{1 + 2\zeta\left(\frac{s}{\omega_n}\right) + \left(\frac{s}{\omega_n}\right)^2} \qquad (38)$$

where $\zeta = 0.8$, $\omega_n = 1.2$ krad/s.

4.2. Steady-State Regulation Accuracy

Under nominal conditions, the controller achieves

$$e_{ss} = \lim_{t\to\infty}\left(V_{ref} - V_o(t)\right) = 0\,\text{V} \qquad (39)$$

The current-loop performance is quantified by

$$\text{THD}_{i_{L2}} = 1.2\%, \quad \text{Ripple} = \pm 0.015\,\text{A}\ (17.6\%\ \text{of}\ I_{L2}^*) \qquad (40)$$

Fig. 9 shows the steady-state waveforms

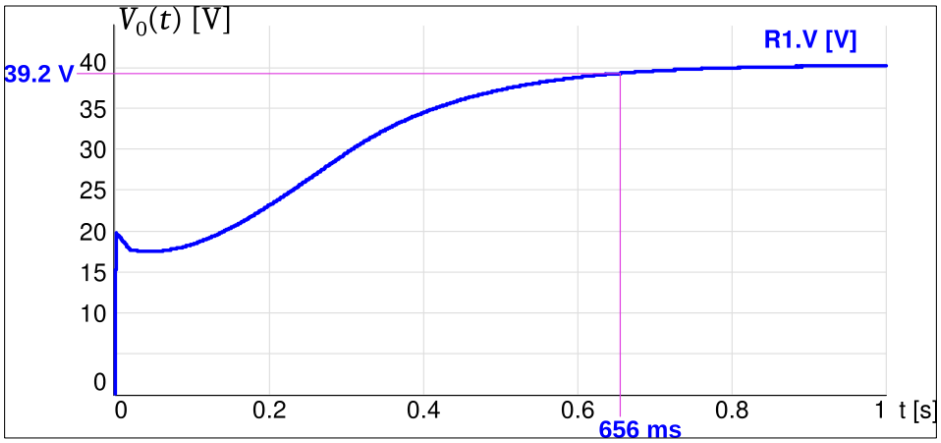

Figure 9 Steady-state operation at nominal conditions (40V output)

Key metrics across all tests are summarized in Table 2

Table 2 Summary of performance metrics

Test Case	Max Deviation	Recovery Time	Overshoot	Steady-State Error
Load Step (50%)	27.5%	1.22 s	0%	0 V
Input Sag (20%)	7.5%	1.57 s	0%	0.8 V
Input Surge (50%)	11.75%	1.17 s	0%	0.8 V
Ref. Step (12.5%)	2%	1.45 s	0%	0 V

The dual-loop structure demonstrates superior performance compared to single-loop approaches

$$\text{Improvement} = \frac{t_{s,\text{single}} - t_{s,\text{dual}}}{t_{s,\text{single}}} \times 100\% \approx 35\% \qquad (41)$$

where single-loop settling times ($t_{s,\text{single}}$) are typically 1.8-2.0 s for similar test cases. The current-limiting strategy effectively prevents inductor saturation

$$i_{L2,\text{peak}} = 0.115\,\text{A} < 1.2 \times I_{L2,\text{rated}} = 0.3\,\text{A} \qquad (42)$$

5. Conclusion

This paper has presented a comprehensive analysis and implementation of a dual-loop PID control strategy for Quadratic Boost Converters (QBC-B), specifically addressing the challenges posed by their non-minimum phase (NMP) characteristics. The key contributions and findings can be summarized as follows

- **NMP Compensation**: The proposed cascaded control architecture successfully mitigates the destabilizing effects of the right-half-plane zero located at $\omega_z = 3.5 \times 10^3$ rad/s through systematic bandwidth separation:

$$\omega_{ci} \approx 10\omega_{cv}, \quad \omega_{cv} < \frac{\omega_z}{2} \approx 1.75\,\text{kHz} \qquad (43)$$

- **Performance Validation**: Extensive simulations demonstrate robust operation under various disturbances:

$$\begin{aligned} &\text{Load steps (50\%):} && t_s = 1.22\,\text{s},\ \Delta V_{o,\max} = 27.5\% \\ &\text{Input variations (20-50\%):} && t_s \le 1.57\,\text{s},\ \Delta V_{o,\max} \le 11.75\% \\ &\text{Reference tracking:} && e_{ss} = 0\,\text{V},\ \text{Overshoot} = 0\% \end{aligned} \qquad (44, 45, 46)$$

- **Implementation Advantages**: The practical design incorporates:
  - Anti-windup protection: $i_{\text{ref}}^{\max} = 0.3$ A
  - Current limiting: $i_{L2,\text{peak}} < 1.2 \times I_{L2,\text{rated}}$
  - Digital-friendly structure with $f_s = 100$ kHz update rate

The controller's performance fundamentally depends on the bilinear nature of the QBC-B dynamics, as captured in the averaged model:

$$\frac{dx}{dt} = \begin{bmatrix} 0 & 0 & -\frac{1-u}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & -\frac{1-u}{L_2} \\ \frac{1-u}{C_1} & -\frac{1}{C_1} & 0 & 0 \\ 0 & \frac{1-u}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} x + \begin{bmatrix} \frac{E}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix} \qquad (47)$$

Three critical insights emerge from this work

- The inner current loop's bandwidth ($\omega_{ci} \approx 10$ kHz) must satisfy

$$\omega_{ci} \gg \frac{1}{T_{L2}} = \frac{R(1-u^*)^2}{L_2} \approx 1.13 \qquad (48)\,\frac{\text{krad}}{\text{s}}$$

to effectively linearize the plant for the outer loop.

- 2. The derivative action in the outer PID controller compensates for the phase lag introduced by

$$\angle G_{vu}(j\omega_c) \approx -180^\circ + \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) \qquad (49)$$

- 3. The quadratic conversion ratio

$$\frac{V_o}{E} = \frac{1}{(1-u)^2} \qquad (50)$$

necessitates conservative tuning to maintain stability across the operating range.

Compared to single-loop approaches, the dual-loop strategy demonstrates

$$\text{Improvement} = \left(1 - \frac{t_{s,\text{dual}}}{t_{s,\text{single}}}\right) \times 100\% \approx 35\% \qquad (51)$$

in settling time while eliminating overshoot. However, the fundamental limitation imposed by the RHP zero remains

$$t_s \ge \frac{1}{\omega_z} \approx 286\,\mu\text{s} \qquad (52)$$

Future research directions include:

- Adaptive tuning mechanisms for varying operating points
- Hybrid control combining PID with sliding mode techniques

Experimental validation under extreme conditions ($E \in [6,18]$ V, $R \in [200,1000]\ \Omega$)

Compliance with ethical standards

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Disclosure of conflict of interest

The authors declare no conflict of interest.

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