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(RESEARCH ARTICLE)

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High-precision sensor front-end: Multi-path op-amp with chopping and nested miller compensation

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Abstract

We introduce a low-noise, dual-path op-amp for precision sensing. Chopping lifts. During the chopping process, the circuit translates the low-frequency offset and flicker (1/f) noise components out of baseband and repositions them around the chopping sidebands commonly referred to as the chop band. A dedicated feedback path commonly called the ripple-reduction loop (RRL) detects the periodic ripple and drives a corrective signal that cancels it, thereby strongly attenuating the ripple component. To prevent an RRL-induced notch in the transfer, the signal is steered through two tracks: a low-frequency path (LFP) and a high-frequency path (HFP). The LFP pairs chopping with the RRL to keep the low band clean, while the HFP terminates in a class-AB output stage for improved energy efficiency under dynamic loading. A nested Miller compensation scheme (NMC) couples the two paths, yielding an approximately first-order closed-loop response over the intended bandwidth.

The prototype is implemented in 180 nm 1P6M CMOS, operates from 1800 mV, dissipates 174 µW, and occupies 0.0118 cm^2 of active area. The measured UGBW is 3160 kHz.

Keywords: Amplifier; Nested Miller Compensation; Current-Feedback Instrumentation Amplifier; Input-Referred Noise

1. Introduction

The surge in Internet-of-Things (IoT) deployments has created demand for a wide range of sensors. In that landscape, MEMS devices are appealing for their small footprint, strong SNR, and favorable cost [1–3]. Because their output currents and voltages are tiny, the saturated iron-core superconducting fault current limiter (SISFCL) [4]. significant amplification is necessary at the interface; as a result, the front-end op-amp must offer very large gain, present an exceptionally high input impedance to the source, and exhibit a low noise floor, thereby preserving signal fidelity and minimizing loading on the preceding stage. to ensure reliable readout [5–7].

Two well-established strategies are used to push the noise floor down: chopping and auto-zeroing [8]. Auto-zeroing operates in two steps: first, capturing offset and 1/f components on a capacitor, then subtracting them—so it is inherently discrete-time and introduces switching artifacts and folded high-frequency noise, which can be problematic for continuous-time operation. Chopped front ends, by contrast, are a better fit for continuous-time, low-power/low-noise front-end use cases [9].

Under chopping, the offset and 1/f terms are shifted by the chopper frequency (fchop), leaving mostly thermal noise in baseband but also creating ripple. By integrating the ripple observed at the output, the RRL drives input-side cancellation to suppress it [10]. The trade-off is that the RRL can introduce a notch around fchop, trimming bandwidth.

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To avoid that penalty, the amplifier routes signals through dual channels—LFP handling low frequencies, HFP handling high. Nested Miller compensation (NMC) then blends their responses so the closed-loop behavior is effectively first-order across the band [11].

Over the specified bandwidth, the integrated loop is well modeled as first order. [11]. The HFP terminates in a class-AB output stage to keep power draw modest under dynamic loading.

Silicon summary. Built in 180 nm 1P6M CMOS, powered at 1800 mV, dissipating 174 µW, with an active area of 0.0118 cm^2. Measured UGBW = 3160 kHz and input-referred noise = 0.0118 µV/√Hz, yielding NEF = 4.46.

2. Realization of the Dual-Path (LFP/HFP) Amplifier

Figure 1 lays out a two-branch signal flow: a red-coded HFP and a blue-coded LFP. The LFP is deeper, using four gain stages; the HFP is lighter with two.

Inside the LFP, chopping knocks down offset and 1/f noise; the RRL completes the job by reducing the ripple. left by chopping. For additional cancellation, the current adder drives A6 against A2 with opposite polarity.

The branches are shaped to complement each other in frequency. The HFP behaves like an exhibit first-order dynamics set by Cm1; the LFP shows second-order dynamics with poles at Cm1 and Ci1. Nested Miller compensation (NMC) then blends the two responses into a stable overall loop.

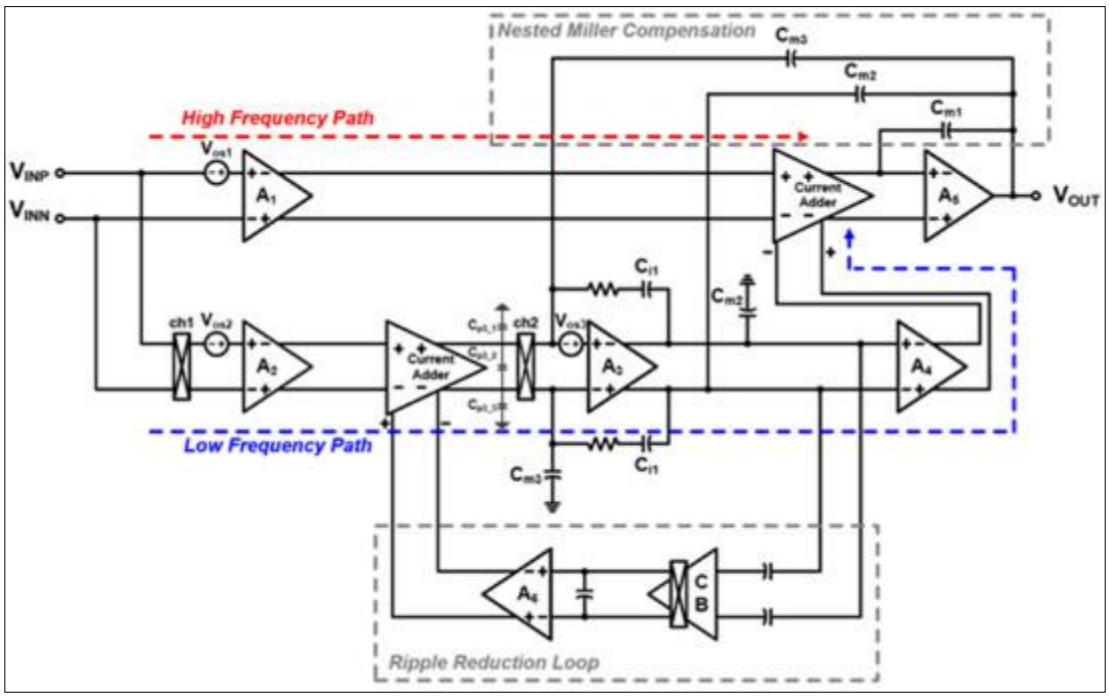

Figure 1 Proposed amplifier architecture featuring chopping and nested Miller compensation

2.1. LFP Structure and Noise Handling

Figure 2 highlights LFP, built from four cascaded stages (vs. two in the HFP), largely governs offset and 1/f noise. Chopping translates the offset away from baseband and flicker components into the chopping band, reducing their footprint in the baseband.

Figure 3 depicts the input section. The current-summing stage uses a common-mode feedback (CMFB) scheme realized as a closed loop around an auxiliary amplifier. Within this loop, the node labeled Vcmfb serves as the control point that governs the adder's output common-mode level and directs the loop's corrective action.

held at ½ VDD, which fixes the output common-mode levels Vop and Von at ½ VDD.

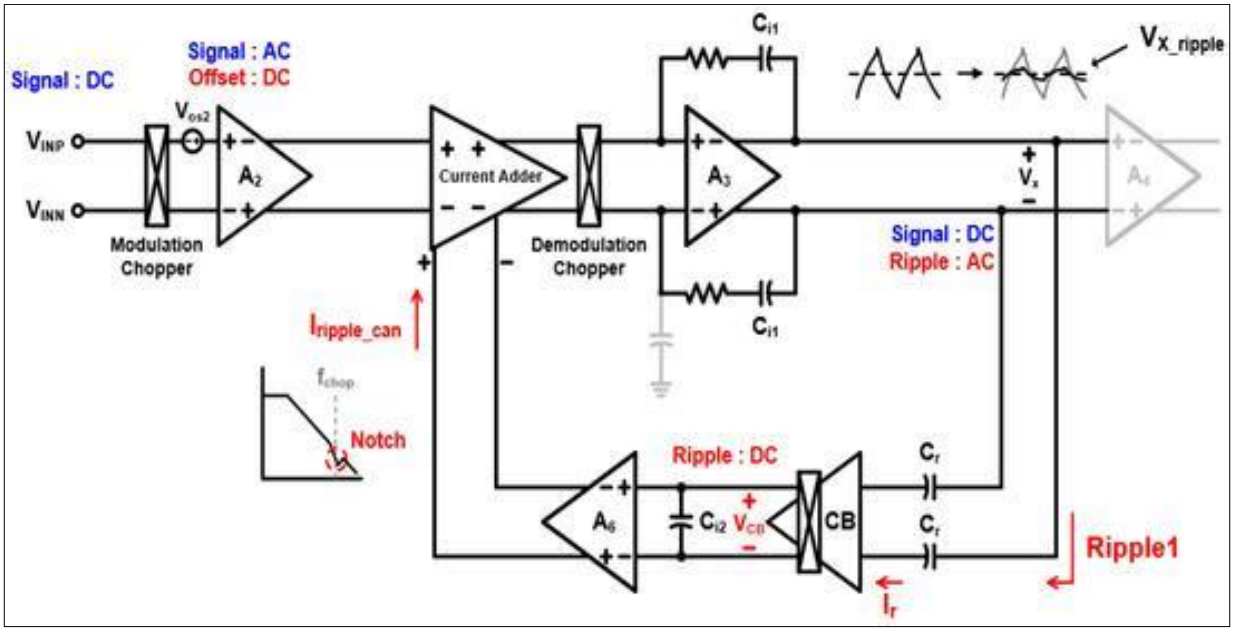

Figure 2 LFP block diagram highlighting the ripple control loop (RRL)

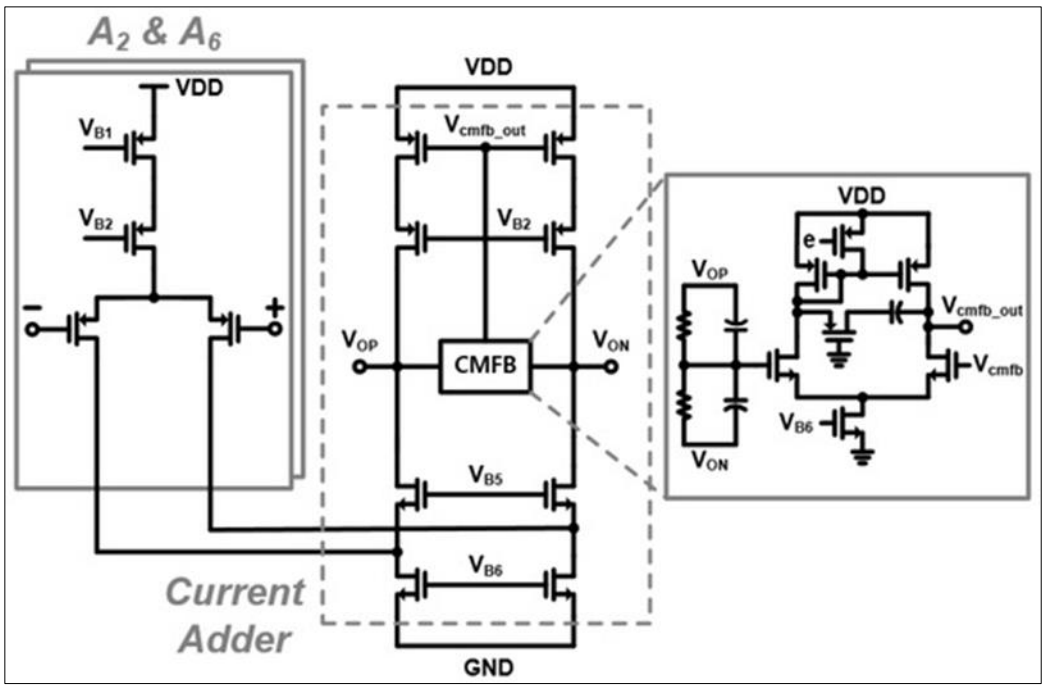

Figure 3 Input front-end circuitry for the low-frequency path

2.2. Ripple Cancellation Loop: Concept and Implementation

A2 turns the incoming voltage into a current, while A6 does the same for the ripple component. Those two currents hit the current adder with opposite polarity, so their difference knocks the ripple down. The adder's output current is integrated by A3, creating the node voltage Vx. Then A4 converts Vx back to a current, which is summed with the High-Frequency Signal Path current at the adder ahead of A5.

The demodulating chopper, working with the A3 integrator, acts on A2's offset and imprints a ripple at Vx. Here, Gm2 denotes the A2 transconductance parameter, and fch is the chopper frequency. The ripple at the A3 output is

Vrip1 ≈ (Vos2 * Gm2) / (2 * Ci1 * fch).

If A4 has transconductance Gm4, further integration by A5 produces the output ripple

Vrip2 ≈ (Vrip1 * Gm4) / (8 * Cm1 * fch).

To cut the ripple even more, the ripple-reduction loop is enabled. (RRL) is activated is engaged. The AC term Vrip1 passes through the coupling capacitor Cr, generating a current Ir given by

|Ir| ≈ 2 * Cr * fch * |Vrip1|,

which then drives the current buffer (CB). Provided current sources M1, M2, M7, and M8 have high output impedance, the CB follows

Vcb = |Ir| * Rcb with Rcb = Acb / (2 * Cr * fch),

Here, Acb denotes the DC gain produced by the NMOS cascode stage inside the CB block; in other words, it captures the steady-state amplification contributed by that cascode section. the CB. Routed through A6, this action yields an estimate of the cancellation current

IripCan ≈ (Acb * Gm2 * Gm6 * Vos2) / (2 * Ci1 * fch).

With a 10 mV injected offset at Vx (Figure 5), the trace without RRL (red) shows about 68 mV of ripple, while enabling RRL (blue) reduces it to 8 mV, an ≈88% cut. The ripple-suppression factor is

F = IripCan / Ios2 = (Acb * Gm6) / (2 * Ci1 * fch), with Ios2 = Vos2 * Gm2.

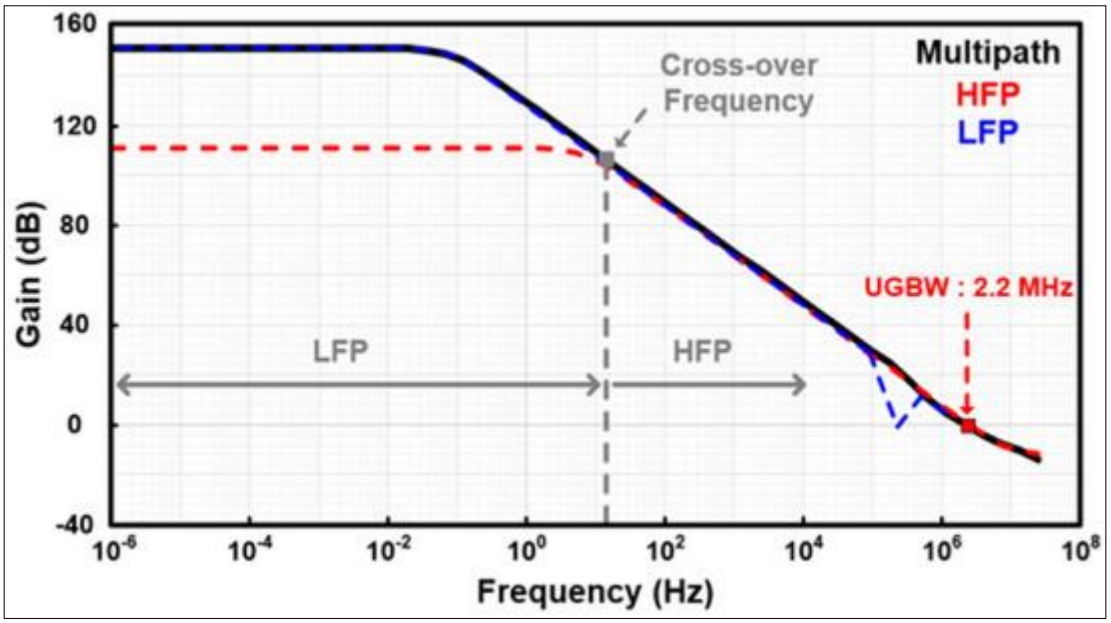

Figure 4 Bode magnitude/phase of the proposed design (simulation)

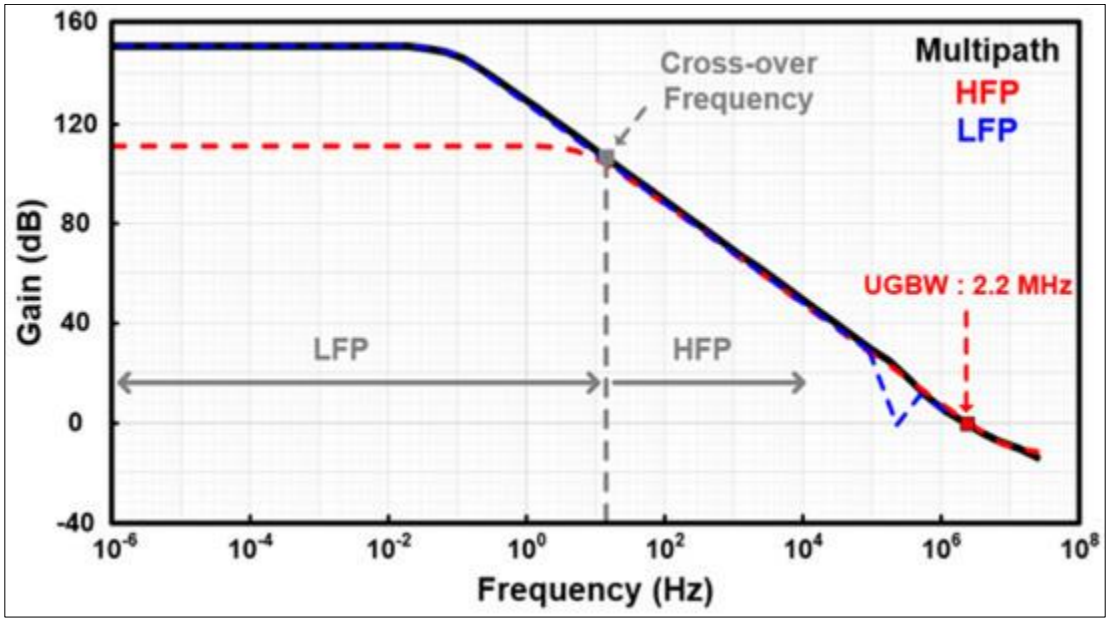

Figure 5 Bode magnitude/phase of the proposed design (simulation)

2.3. Remaining Input Offset: Diagnosis and Design Fixes

In the LFP, chopping together with the RRL suppresses both offset and 1/f noise—if F is large, any remaining ripple fades to near zero. If F is large, any residual ripple is essentially negligible. By contrast, the HFP does not employ chopping, so its input offset is not canceled and shows up as the input's residual offset

The portion of residual input offset attributable to A1's offset (Vos1) is defined by the expression in your derivation (kept unchanged per your rule).

The portion of residual input offset due to A1's offset Vos1 is

VresOff1 ≈ (Ah / Al) * Vos1,

where Ah and Al are the HFP and LFP gains, respectively [14].

Another contribution comes from A3's offset Vos3. Chopper ch2 converts Vos3 to a square wave and, through parasitics Cp31–Cp33, drives an AC current set by A2's AC input [14]. Chopper ch1 then translates that AC term into a DC offset:

VresOff2 ≈ 4 * Vos3 * fch * Cp3 / Gm2,

with Cp3 = Cp31 + Cp32 + Cp33.

Finally, ch2 uses four CMOS switches (Figure 8). Clock-feedthrough mismatch between Cpch21 and Cpch23 introduces an error that appears as an input offset [14]. The associated term is

VresOff3 ≈ 2 * dCpch2 * Vclk * fch / Gm2,

where dCpch2 = Cpch21 − Cpch2.

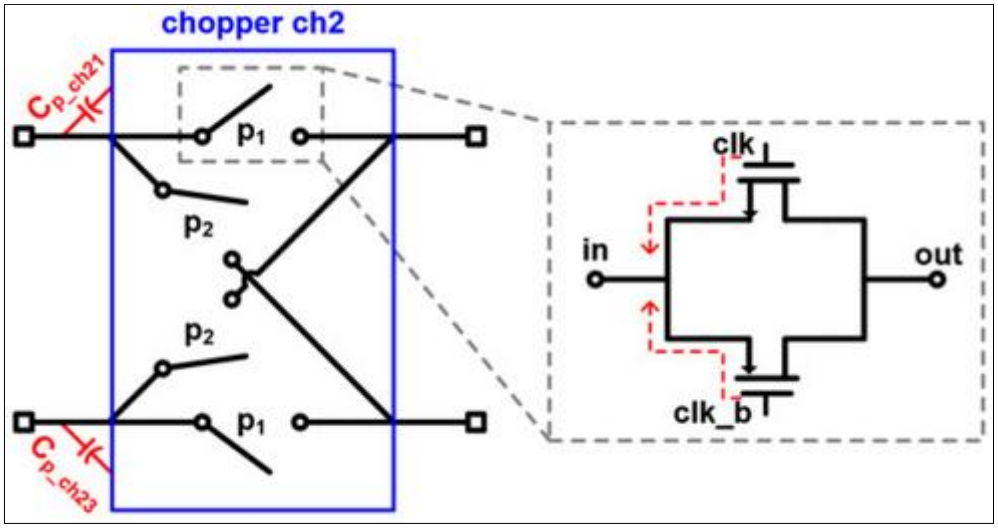

Figure 6 Schematic of one of the ch choppers

3. Bench Results and Metrics

3.1. Core of Building the Chip and Experimental Setup

To validate the concept, we realized the multi-path operational amplifier as a silicon prototype manufactured in a conventional 180 nm CMOS technology node, enabling direct hardware evaluation of the design. 180 nm CMOS node. Figure 9 pairs a die shot with the bench hardware. Running from 1800 mV, the device dissipates 174 µW and occupies 0.0118 cm^2 of active silicon.

For evaluation, the die was wire-bonded to a PCB. The clock and input were sourced from a waveform generator, the output traces were logged by a digital oscilloscope, and a dynamic signal analyzer handled the spectrum measurements.to obtain spectral measurements.

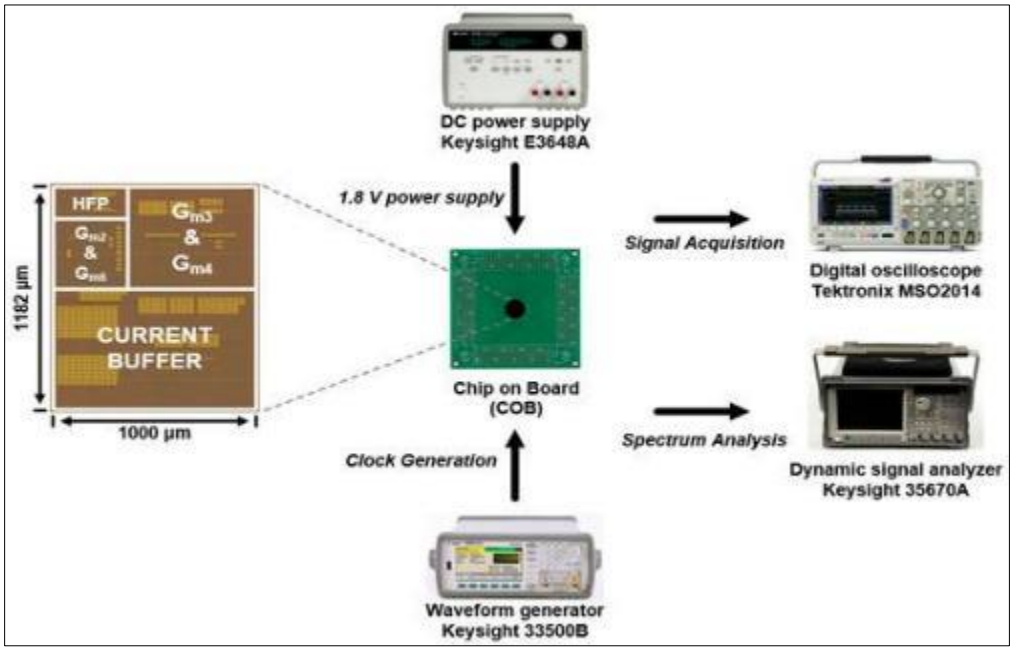

Figure 7 Chip micrograph and the laboratory test-and-measurement bench used to characterize and verify the proposed multi-path amplifier, including the instrumentation and fixtures used during evaluation

3.2. The Result of Bench and Metrics

Using sinusoidal (a) and pulsed (b) stimuli, we evaluated the buffer behavior (Figure 10). For the sine case, the oscilloscope was set to 0.4 ms/div horizontally and 200 mV/div vertically. For the pulse case, the settings were 0.002 ms/div (timebase) and 50 mV/div (vertical). In both tests, the input (red) and output (blue) trace a 100 mV drive into a 0.05 nF load. The measured pulse rise time is 0.00115 ms.

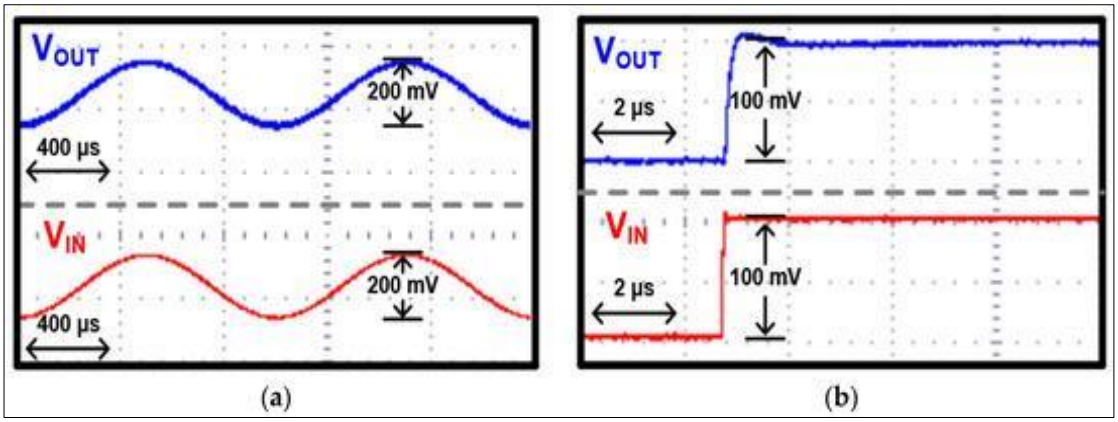

Figure 8 Buffer operation measurement results: (a) sine wave response, (b) pulse wave response

See Figure 11 for the slew check: the output (blue) tracks the input (red) step. The computed slew rate is

Slew Rate = dVout/dt = 1000 mV / 0.00115 ms ≈ 8.70×10^5 mV/ms.

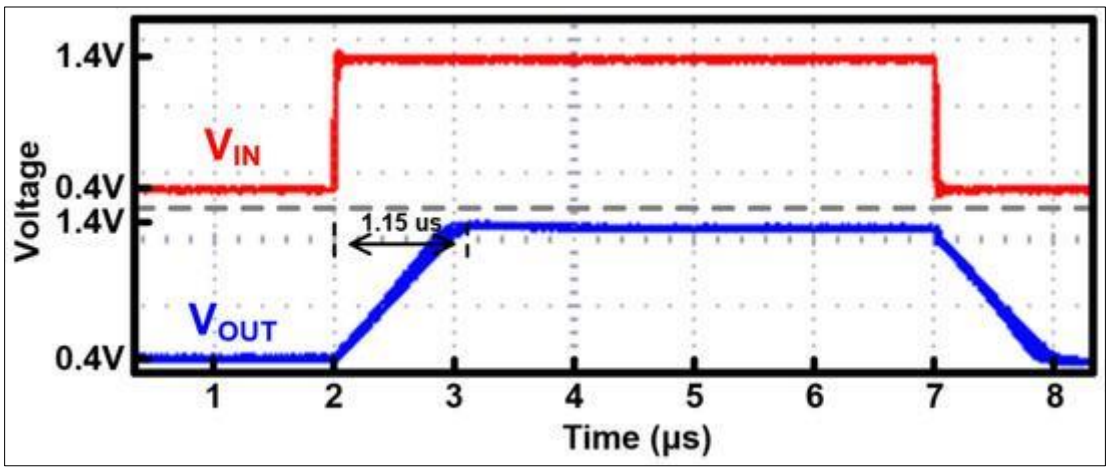

Figure 9 Slew rate measurement results

Figure 12 shows the open-loop sweep. The amplifier delivers a 135 dB DC gain, and the magnitude falls with a first-order slope coming in at 50 dB at 10 kHz and crossing unity at 3160 kHz (UGBW). The measured trace lines up well with the simulated curve in Figure 7.

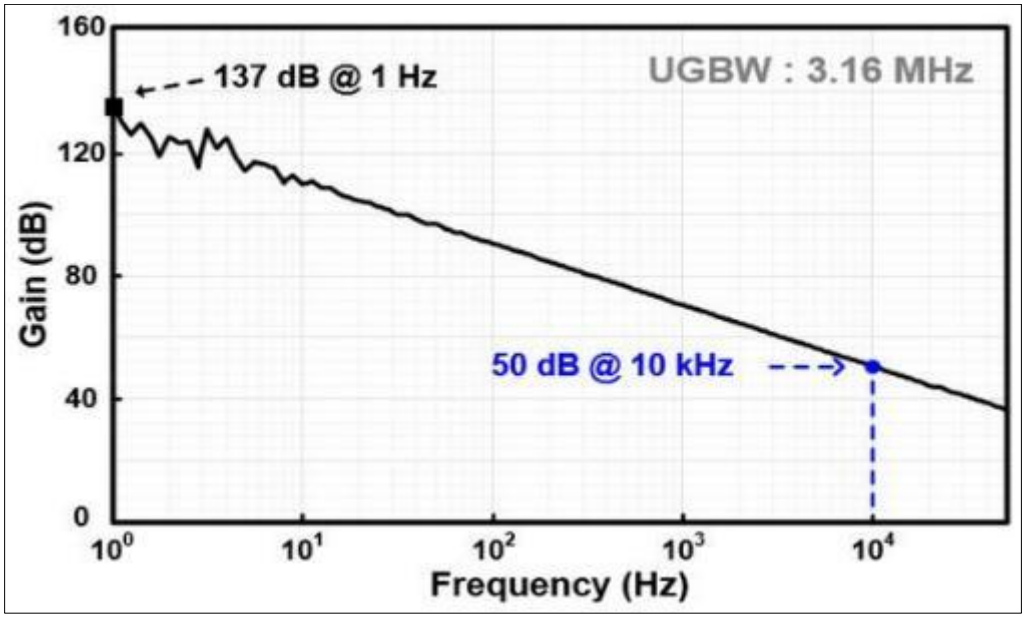

Figure 10 Open-loop gain measurement for the presented amplifier

Figure 13 compiles the rejection data. At 0.001 kHz, the amplifier posts CMRR = 125 dB and PSRR = 100 dB. Over the sweep, the worst-case values are 69.8 dB for CMRR and 71.7 dB for PSRR.

Figure 14. Input-referred offset across samples statistics across multiple samples: the average offset is 0.00199 mV, and the lowest value to the highest spread is 0.00373 mV.

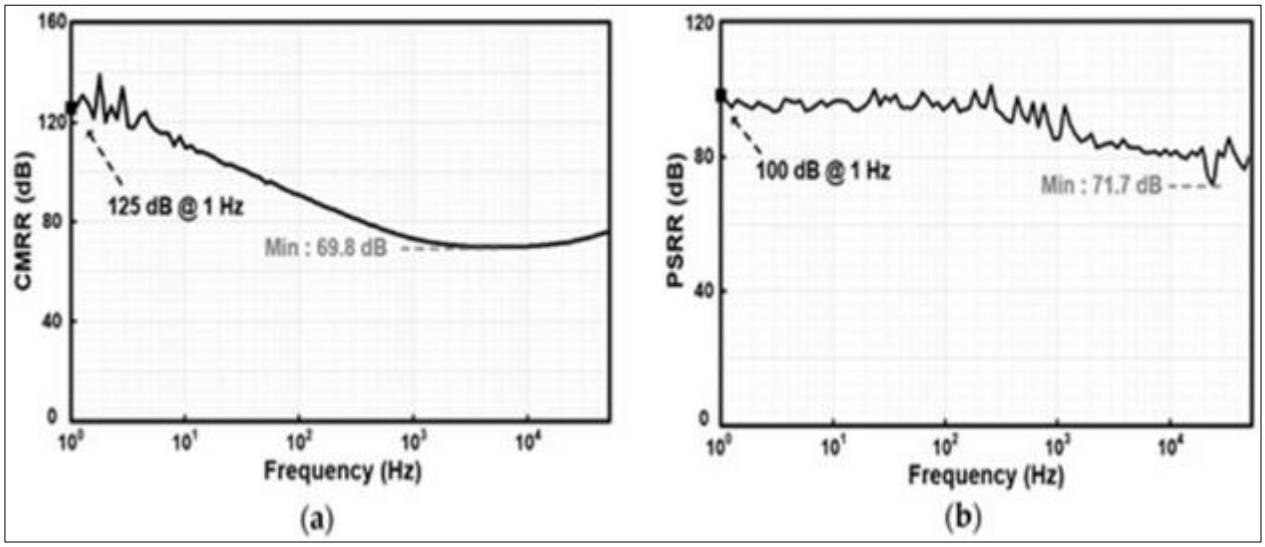

Figure 11 Measurement results for (a) CMRR and (b) PSRR

Figure 14 captures the input-referred offset results. Across the sample set, the mean offset is 0.00199 mV, and the peak-to-peak spread is 0.00373 mV.

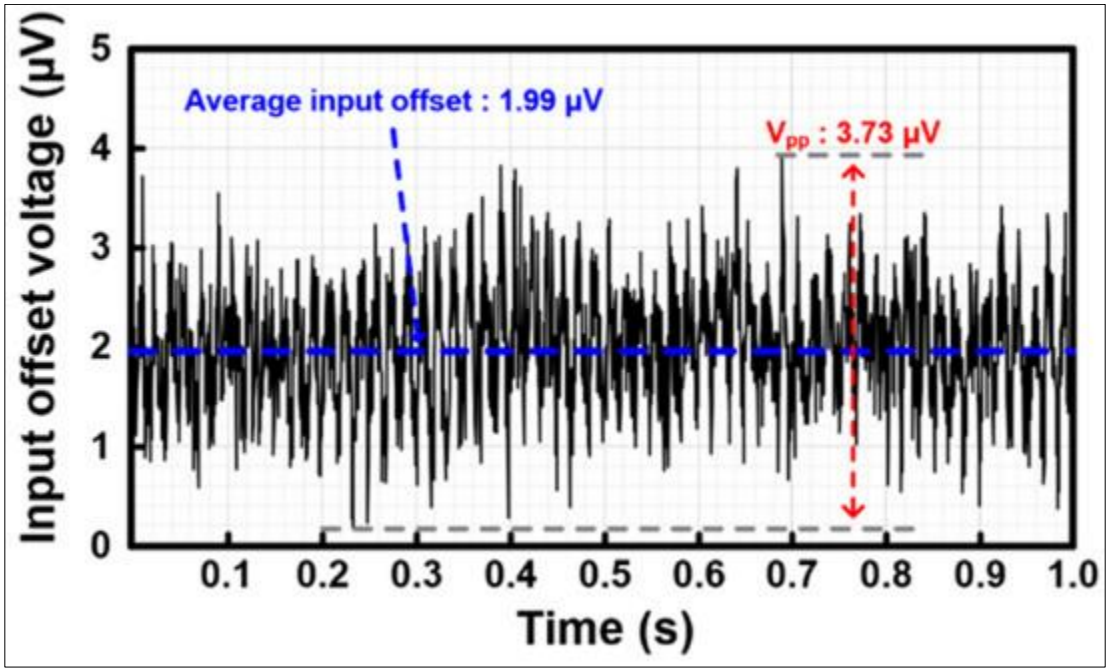

Figure 12 Statistical distribution of the input-referred offset

Noise was swept from 0.0005 kHz to 0.2 kHz (Figure 15). In Figure 15a, the input-referred noise density comes in at 0.0478 µV/√Hz at 0.001 kHz and 0.0108 µV/√Hz at 0.2 kHz. The histogram in Figure 15b—taken at 0.2 kHz across 10 samples—yields an average of 0.0118 µV/√Hz.

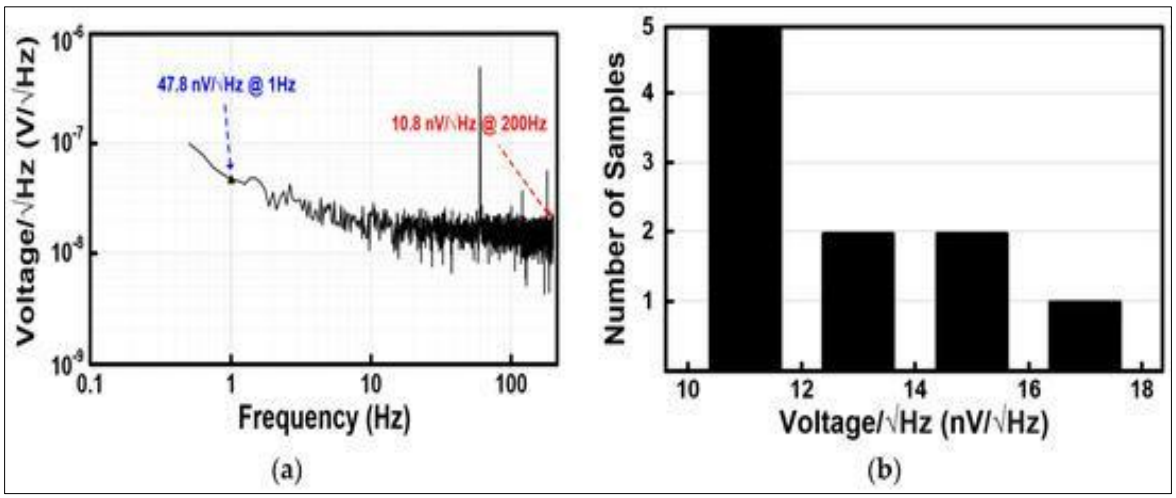

Figure 13 Noise measurement results: (a) input-referred noise density, (b) histogram of noise at 200 Hz

4. Discussion

To stack this design against prior low-noise amps, we use the factor the noise efficiency (NEF) defined as NEF = Vni * sqrt ((2 * Itot) / (π * UT * 4 * k * T * BW)) [15].

The prototype draws 0.0967 mA from 1800 mV, reaches UGBW = 3160 kHz, and posts input-referred noise = 0.0118 µV/√Hz, which together yield NEF = 4.46. While the multi-path approach costs more area and power than some simpler options, it buys a stronger noise–bandwidth trade-off that drives this result.

5. Conclusion

We built a chopper-stabilized, two-path op-amp with nested Miller compensation for precision sensing. Chopping plus the RRL knocks down offset, 1/f noise, and ripple; the LFP/HFP split preserves bandwidth; and the compensation keeps the loop well behaved.

Made in 180 nm CMOS, the design uses 0.0118 cm^2 of silicon and dissipates 174 μW. It posts a slew rate of 8.60×10^5 mV/ms, DC gain > 137 dB, CMRR > 125 dB, and PSRR > 100 dB. With input-referred noise = 0.0118 μV/√Hz and UGBW = 3160 kHz, the amplifier reaches NEF = 4.46, making it a strong fit for demanding precision-sensor interfaces.

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