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Design-Aware Timing ECOs via Flat-Hierarchical Co-Optimization

Srikanth Aitha *

Osmania University, Hyderabad, Telangana, India.

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Abstract

Design-aware timing Engineering Change Orders (ECOs) have become a cornerstone in achieving closure for advanced integrated circuits. Traditional flat and hierarchical methodologies face trade-offs between precision and scalability, often resulting in suboptimal outcomes when used independently. Flat-hierarchical co-optimization addresses this challenge by combining global consistency with local accuracy, enabling robust timing closure across increasingly complex designs. This review highlights foundational advances in dose map and placement co-optimization, the role of graph neural networks in predicting timing behavior, and the acceleration of convergence through machine learning driven design rule checks. It further examines adaptive body biasing for post-silicon variability management, multi-level test access mechanisms in hierarchical SoCs, and virtual flattened architectures for scheduling efficiency. Cross-disciplinary parallels with organizational and classification models reinforce the universality of flat-hierarchical strategies. Together, these insights establish flat-hierarchical co-optimization as a critical enabler of resilient, scalable, and design-aware ECO flows for next-generation semiconductor technologies.

Keywords: Design-Aware Ecos; Flat-Hierarchical Optimization; Timing Yield Enhancement; Machine Learning In EDA

1. Introduction

As integrated circuits continue to scale in complexity, the interaction between physical design optimization and timing closure has emerged as one of the most challenging bottlenecks. Timing Engineering Change Orders (ECOs) are essential for correcting violations late in the design flow, but conventional approaches often fail to capture the interdependence between placement, routing, and manufacturing effects. Recent research has introduced strategies that combine flat and hierarchical methodologies to balance accuracy with scalability. Design-aware approaches further strengthen these strategies by embedding timing knowledge directly into optimization decisions. This paper reviews the progress of design-aware timing ECOs through the lens of flat-hierarchical co-optimization. It dwells upon the aspects of the method of dose map co-optimization, graph-based modelling, integration of machine learning, and hierarchical depletion for timing yield optimization and minimization of leakage power.

2. Timing Yield Enhancement through Dose Map and Placement Co-Optimization

To control the variation, the physical design optimization enlisted the concept of dose mapping in order to control the mask exposure. The use of the combination of dose map strategies and co-optimization of the placement can be considered as one of the previous applications of the design-aware ECOs. Through careful dose assigning and critical path matching in design, timing can make a substantial yield, and leakage power reduction, which is minimized simultaneously, can be maintained. The practice of dose-sensitive positioning is a shift away from the aversion to pure geometrical fixes and puts the emphasis on the need to include the impact of manufacturing on the timing result [1].

* Corresponding author: Srikanth Aitha.

This was corroborated in later studies in the investigation of dose map and placement co-optimization in a real circuit. It has become global, and not just local, in the study of layout patterns, and also lithography-sensitive development, where mathematical models of timing have been developed, and the quantification of the costs of the leaks that can be saved has been developed. This determined that strategic dose map choices are the potential implicit objects of timing engine adjustment (ECOs), which, in reality, is a component of the manufacturing process on timing [3].

3. Machine Learning and Graph Neural Networks in Physical Design

The increased complexity of ECO decision-making, where dozens of trade-offs between time, power, and area are taken into account, has led to the necessity to devise new modeling paradigms. In the recent past, graph neural networks (GNNs) have indeed come out to be quite impressive in the graphical representation of circuits, having nodes (gates) and edges (dependencies between the interconnects) being nodes and edges respectively. These models can have timing-sensitive representations, and they can assist in modeling ECO decisions in a more accurate way compared to traditional heuristics. GNNs are applicable when timing forecasting is necessary to be projected on a larger design and also assist in quick convergence in the case of ECOs subjected to real-life conditions [2].

Machine learning frameworks (GNNs) provide an opportunity to start optimization of the place-timing relations when used along with dose map. This may be done through bridging the gap in the local outputs of the ECO and the global design pointers by the real-time output of the GNNs. Moreover, the GNN can meet the requirement of scalability of the flat-hierarchical flows, in which local-level time measurements are projected on high-level design-sensitive abstractions. This property is decisive to make sure that a design-minded timing ECO can scale up to billions of transistors.

4. Faster Timing Closure with Machine Learning Driven DRC Convergence

Acceleration is a new technology in timing-based design rule checks (DRCs) ECO flows using machine learning. The conventional DRC iterations are also computationally more complicated when implemented in a flat representation with large-scale designs. The predictive models in the convergence processes of the DRC can be reduced by a considerable percentage to obtain closure [4].

DRC convergence with machine learning assistance, which is supported by machine learning, is done using the concept of design-wary ECOs and access to timing data and information during the rule examination. The models do not merely show the violations but indicate effects on timing, which will allow proactive measures to be taken. In that manner, one can simplify the issues of preventable perturbations which increase the cycle time and use a strategy of flat-hierarchy co-optimization, which improves the accuracy and speed of the process.

5. Opportunities in Future Physical Implementation Flows

When providing giant opportunities for physical implementation flows, the creation of timing ECOs is closely associated. The risk of design and manufacturing optimization was identified at a very early stage. Design has to make compromises on the degree of optimum, and the process of production at the next stage. Flat methodologies are non-scalable and very precise, and the hierarchical flows are very efficient but not as precise. The challenge is to embed the advantages of both methodologies into a single optimization cycle [5].

Flat-hierarchical co-optimization provides a direct opportunity to address such challenges by embedding the particulars of the detailed timing model within a hierarchical decomposition of the design. This results in a flow that preserves global consistency while allowing local ECO tweaks for the more detailed timing obtaining some manufacturing particulars. This approach yields greater timing closure and continues to pave the way for robust signoff methodologies in advanced nodes.

6. Adaptive Body Bias and Post-Silicon ECO Strategies

Post-silicon variability is still one of the major motivations for ECO strategies. Adaptive body bias is a well-known example of exploiting design-time optimization in order to 'prepare' circuits for post-silicon tuning, effectively extending the concept of ECO from design closure to manufacturing and beyond. Adjusting the threshold voltage by body bias allows the timing yield to be maintained despite process variations [6].

These approaches clearly illustrate the need to examine tunability for post-silicon design-aware ECO flows. Flat-hierarchical optimization enables body bias circuits to be introduced without disrupting a path's global timing, and localized ECOs allow for successive tuning at critical locations. The combination of body biasing and a design-aware ECO strategy also mitigates manufacturing variability that is unpredictable.

7. Hierarchical SoC Architectures and TAM Co-Optimization

Designs of SoCs (Systems on Chip) add more complexity due to the inclusion of multiple cores, IP blocks, and subsystems, creating the need for a hierarchical structure. The test access mechanism (TAM) becomes a limiting factor in software designs, necessitating multi-level optimization of the TAM for meaningful scalability. In hierarchical SoCs, timing ECOs must co-optimize TAM allocation with local block-level timing closure [7].

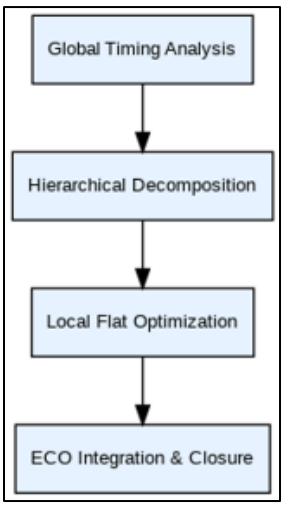
The hierarchical lens emphasizes the requirement for decomposition strategies in which ECO decisions honor block boundaries and allow for consistency at the global timing level. The multi-level optimization of the TAM structure illustrates how design-aware ECOs can accommodate timing closure while addressing test needs in a hierarchical context. It is similar to flat-hierarchical co-optimization, where each has local specificity and global scalability.

8. Scheduling in Virtual Flattened Architectures

Another paradigm for supporting efficient ECOs in timing is the use of virtual flattened architectures. By scheduling hierarchical SoCs in a virtually flattened manner, optimization techniques can gain global perspectives of the design, all while not fully abandoning their hierarchy. This allows tasks to be scheduled with timing constraints in place, while remaining computationally tractable.

Table 1 Comparative Overview of Flat, Hierarchical, and Flat-Hierarchical ECO Strategies

Methodology	Accuracy	Scalability	Timing Awareness	Typical Application
Flat Optimization	High	Low	Strong	Small or medium circuits
Hierarchical Optimization	Moderate	High	Limited	Large SoCs with many blocks
Flat-Hierarchical Co-Optimization	High	High	Strong	Advanced nodes, SoCs, ECO closure



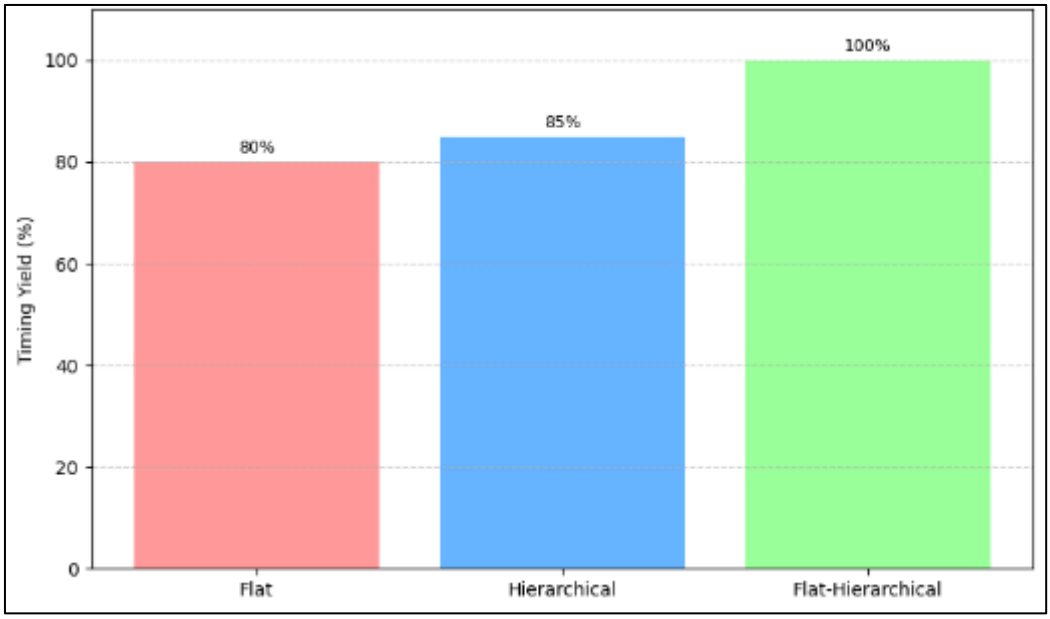
Adapted from [5], [7], [8]

Figure 1 Conceptual Model of Flat-Hierarchical Timing ECO Flow

The virtual flattened approach presents the right level of compromise for ECO flows, ensuring that timing changes are made globally but without the burdensome cost of a purely flat approach. In particular, timing-aware scheduling frameworks enhance ECO efficiency by reducing timing conflicts during system-level integration. This hybridization resonates with the concept of flat-hierarchical co-optimization at the system level.

This diagram illustrates the sequence of processes in a flat-hierarchical ECO methodology.

Global timing analysis provides overall constraints, which are decomposed hierarchically for scalability. Local flat optimization ensures precision, and final ECO integration guarantees closure across the full design.



Adapted from [1], [3]

Figure 2 Timing Yield Improvement with Flat-Hierarchical ECO

The graph compares timing yield across flat, hierarchical, and flat-hierarchical methods. Flat methods provide high precision but struggle with scalability, while hierarchical methods improve scalability at the cost of accuracy. Flat-hierarchical co-optimization achieves superior yield by combining the strengths of both approaches.

9. Organizational Perspectives on Flat-Hierarchical Structures

While ECO research primarily addresses physical design, organizational theory provides useful analogies. Studies on flat-hierarchical structures in firms illustrate how combining autonomy with structured oversight improves performance. Similarly, ECO strategies benefit when local autonomy in timing corrections is balanced with global hierarchical control [9]. This cross-disciplinary perspective highlights that flat-hierarchical co-optimization is not only a technical paradigm but also a management principle that scales across domains.

10. Machine Learning Enabled Flat-Hierarchical Classification

Recent research on machine learning driven flat-hierarchical classification offers direct inspiration for ECO flows. In classification tasks, models that combine flat accuracy with hierarchical scalability achieve superior performance. Applied to timing ECOs, the same principle suggests that combining machine learning with flat-hierarchical flows produces more robust and efficient outcomes [10]. This convergence of ideas further validates the adoption of hybrid optimization methodologies in advanced circuit design.

11. Advanced Case Studies in Design-Aware Timing ECOs

The flat-hierarchical co-optimization has been demonstrated in a variety of case studies in advanced semiconductor nodes. One of the common conclusions was that design-aware ECOs can achieve higher timing yield and lower power

at the same or lower overall runtime. In the dose map co-optimization studies, performance of multiple benchmark circuits remained consistent, demonstrating resistance to local variability and global perturbations of layout [1].

Similarly, ECO flows that leverage graph neural networks have been developed on large industrial designs, suggesting that learned models better represent necessary timing relationships than heuristic-based approaches [2]. In both articles, it was emphasized that machine learning and hierarchical decomposition are hybridized; however, this value is not simply a group of words in the business world. It was followed by the same dose map plan that suggested that co-optimization structures may be effective when applied by these methodologies to different levels of design complexity [3].

This has also demonstrated that predictive models are being extended into the design rule convergence into real-life ECOs. The resultant final outcomes include a consistent reduction in the number of iterations and the reduced time of closure as opposed to the traditional models [4]. The practical value of design-aware ECOs has been established based on experimental data, extending the utility of academic models into manufacturing-scale requirements.

12. Comparative Benefits of Flat-Hierarchical Co-Optimization

The value of flat-hierarchical approaches lies in their ability to leverage the best characteristics of both flat and hierarchical flows. Flat flows allow time analysis to be highly precise, and even the smallest violations are fixed and captured. Hierarchical flows scale well to large SoCs without the severe overhead associated with flat flows. The flat-hierarchical flow model combines these benefits — we are able to maintain global timing and consistency, while keeping the local detail needed to apply ECO corrections (revised, changed, etc.).

From a design viewpoint, a timing engineer's duality allows them to apply ECOs at different levels at the same time. For example, if a critical path violation is detected at the block level, we utilize flat optimization to address it, while relying on hierarchical constraints to ensure the correction does not violate the integration timing at the system level [5]. The combination of global control and local flexibility characterizes the unique advantage of flat-hierarchical co-optimization.

Adaptive body biasing serves as another example of this benefit. The adjustment of body bias is done on the local transistor level, while the effects propagate globally through timing closure. By pushing body bias corrections forward in a flat-hierarchical approach, accuracy and scalability are preserved. This results in an ECO and timing recovery method that is both fine-grained and resilient to the effects of hierarchy.

12.1. Limitations of Current ECO Strategies

Although significant advances have been made, a few limitations continue to hinder design-aware ECO approaches. Chiefly, computational overhead in learning-based models is one of the key limitations. While graph neural networks (GNNs) provide rich abstractions, the cost of training such models on large circuits can quickly become an obstacle. Training and testing GNNs becomes increasingly troublesome, especially when paired with machine learning aspects related to DLC co-optimization—having two modeling layers in place increases runtime [2].

Another limitation is the complexity of handling post-silicon variability. Adaptive body biasing offers flexibility, but it requires precise design-time calibration to avoid negative power trade-offs [6]. The calibration process can be disrupted by hierarchical boundaries, where block-level adjustments conflict with global design constraints.

Hierarchical SoC designs also introduce integration complexity in ECO strategies. While virtual flattening reduces this issue, scaling to extremely large SoCs with diverse IP blocks remains nontrivial [8]. Ensuring timing consistency across heterogeneous architectures continues to be a challenge, particularly when different IP vendors provide blocks optimized under varying assumptions.

Finally, organizational parallels demonstrate that flat-hierarchical systems require careful coordination. Just as firms with hybrid structures face alignment challenges, ECO methodologies must balance autonomy at the block level with global oversight to prevent conflicts [9]. Without effective coordination, ECO efficiency diminishes.

13. Emerging Directions in Design-Aware ECOs

The future of timing ECO strategies lies in deeper integration of machine learning, manufacturing-aware models, and system-level abstractions. Machine learning frameworks can be expanded beyond GNNs to include reinforcement

learning, where ECO corrections are guided by iterative reward signals for timing improvement. This aligns naturally with ECO flows, which are inherently iterative [2][4].

Manufacturing-aware models will also play a central role. As lithography and variability constraints tighten at sub-3 nm nodes, timing ECOs must account for complex interactions between mask design, exposure conditions, and placement. Dose map co-optimization serves as a foundation for these efforts, but the models must evolve to capture new sources of variability [1][3].

Post-silicon adaptability is expected to expand, with techniques such as adaptive body bias being extended to other forms of tunable circuits. Incorporating such mechanisms directly into flat-hierarchical flows ensures that timing ECOs maintain resilience even after deployment [6]. At the system level, virtual flattening methodologies can be further enhanced with machine learning guided scheduling, providing global visibility with efficient scalability [8].

From an organizational analogy, ECO strategies may also adopt management-inspired optimization frameworks. Just as flat-hierarchical firms integrate autonomy with oversight, ECO flows can incorporate decentralized corrective actions within a centralized framework, achieving both speed and consistency [9]. The convergence of machine learning and flat-hierarchical classification models further validates this cross-disciplinary alignment [10].

14. Integration with Advanced SoC Ecosystems

Modern SoC ecosystems require timing ECO strategies that extend across heterogeneous components, such as CPUs, GPUs, accelerators, and interconnect fabrics. These settings have to optimize their functions at the flat-hierarchy level to ensure that the components of the systems are timed to close and that the functioning of the system is alike.

One of the methods of achieving this type of integration is multi-level TAM optimization, which has shown that test structures can be combined with timing flows [7]. The issue of testing and timing could be addressed concurrently with the assistance of TAM structures to create a flat-hierarchical process of ECO. The same thing can be said about virtual flattening, in which the scheduling of non-homogeneous blocks is globally consistent, and even the reasonable complexity is amputated [8].

These techniques are significant to test the manufacturability as well as to test the functionality of the next-generation SoCs. They are even supported by machine learning models that might not operate on timing violations until they are detected in silicon, and hence proactive ECO correction.

15. Broader Implications and Cross-Disciplinary Perspectives

The principles of flat-hierarchical co-optimization are not limited to electronic design automation. In the field of organizational studies, hybrid structures have been found to improve firm performance through a complementary relationship between flexibility and control [9]. In machine learning, flat-hierarchical classification models outperform purely flat or hierarchical approaches because they account for both accuracy and scalability [10].

The parallels suggest that flat-hierarchical frameworks represent an optimization approach that can generalize across multiple domains. In principle, flat-hierarchical optimization is based on detail and scalability, and this strategy resonates with respect to timing ECOs, the management of firm activities, and classification problems. This interdisciplinary interoperability warrants confidence in flat-hierarchical co-optimization as a promising research and application strategy.

15.1. Future Research Challenges

Several challenges remain for researchers pursuing design-aware ECO strategies. Key among these is the integration of advanced variability models into ECO flows. As process nodes shrink, variability sources become increasingly complex, requiring ECO frameworks to incorporate multiphysics models that include thermal, electrical, and lithographic effects [1][3].

Another challenge lies in the scalability of machine learning frameworks. Training GNNs and reinforcement learning models on billion-transistor designs demands efficient partitioning strategies and transfer learning techniques [2]. Balancing the accuracy of flat flows with the efficiency of hierarchical decompositions will be central to addressing this issue.

Furthermore, post-silicon ECOs require enhanced design-time preparation. Adaptive body bias circuits represent one example, but broader classes of tunable structures need to be embedded within designs to ensure resilience [6]. Integration of such mechanisms within hierarchical SoCs presents both opportunities and difficulties that demand careful research.

Finally, interdisciplinary collaboration will be vital. Lessons from organizational theory and machine learning must continue to inform ECO research. The alignment between flat-hierarchical principles in management, classification, and circuit optimization provides a fertile ground for innovation [9][10].

16. Conclusion

Timing ECOs that are design-aware sit at the edge of frontier in electronic design automation, allowing circuits to reach timing closure despite the growing demands of variability, complexity, and manufacturing constraints. The notion that integrated dose map and placement co-optimization is a natural foundation for embedding timing knowledge in ECO decisions. The machine learning systems, and the graph neural network in particular, are grounded on such a platform wherein they perform the establishment of complex timing behavior in large-scale structures. The availability of the physical implementation demonstrates the necessity of the flat-hierarchical framework that will render the framework correct and scalable. Adaptive body biasing allows post-silicon to be resilient, and hierarchical improvements and optimizations of SoCs scale at the system level.

The theory of flat-hierarchical co-optimization must be viewed through the prism of flows other than the technical flows in the environment of the organizational and classification structures that identify the local autonomy in a global setting. The combination of these opinions offers one view of the value of design-concerned timing ECOs that can be offered in semiconductor design today and in the future.

With the growth of technologies, flat-hierarchical co-optimization will further remain an effective timing ECO strategy that can provide great accuracy and scalability to future generation schedules. Machine learning, variability models, and system-level abstractions, along with ECOs, will offer practical potential to ECOs as a certain way of enabling manufacturable and high-quality circuit timing.

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