World Journal of Advanced Engineering Technology and Sciences
eISSN: 2582-8266
Cross Ref DOI: 10.30574/wjaets
Journal homepage: https://wjaets.com/

(REVIEW ARTICLE)

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CTS-Aware Voltage Scaling Across Distributed Corners: A New Approach to Clock Robustness in Sub-5nm SoCs

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World Journal of Advanced Engineering Technology and Sciences, 2026, 18(03), 047–053

Publication history: Received on 21 January 2026; revised on 01 March 2026; accepted on 02 March 2026

Article DOI: https://doi.org/10.30574/wjaets.2026.18.3.0104

Abstract

The aspect of providing consistently low-energy clock distribution in sub-5nm space has been of high priority, as the processes in which power and requirements have changed with the advent of System-on-Chip (SoC) applications. Conventional methods of scaling voltage without taking into account Clock Tree Synthesis (CTS) are likely to result in timing failures and poor power usage. The current paper presents a discourse on the novel paradigm of CTS-conscious voltage scaling, in which voltage management is tightly combined with clock synthesis and clock allocation policies to provide robustness at the boundaries of distributed processes. It is supported by shift-left methodologies, FinFET-based CMOS technology innovations, scalable silicon architectures, and device-level innovations, including junctionless FishBone FETs. It introduces CTS-conscious voltage scaling as an enabling core service of low-power, high-performance SoCs in advanced nodes by investigating its performance, area, variability, and clock signal integrity consequences.

Keywords: CTS-Aware Voltage Scaling; Sub-5nm Socs; Clock Robustness; Low-Power VLSI

1. Introduction

The inexorable effort to achieve ever-lower power consumption in semiconductor technologies has led to the introduction of sub-5nm System-on-Chip (SoC) architectures. Along with the benefits of enhanced computing efficiency come considerable design and reliability challenges. One of these is clock robustness, especially under Process, Voltage, and Temperature (PVT) fluctuations. The clock system in modern SoCs is no longer merely responsible for coordinating data movement between functional units; it also accounts for a significant fraction of overall chip power, particularly in fast and dense designs.

Clock Tree Synthesis (CTS) applies effectively in this context to reduce timing uncertainties and guarantee signal integrity. However, conventional CTS methods are either too conservative or unsuitable for the high interdependencies of sub-5nm designs. This challenge is further compounded by increased device variation, signal integrity issues, and power delivery limitations. These considerations create a need for dynamic design solutions capable of sustaining reliable clock behavior in continuously varying operating conditions.

CTS-aware voltage scaling presents a strong opportunity to address these challenges. Rather than simply scaling voltage based on CTS-derived timing constraints, this approach accounts for spatial and temporal variations across distributed chip regions. In doing so, it provides a dynamic means to achieve power efficiency without compromising performance or reliability. Such innovation is particularly important in the context of growing design complexity, higher integration density, and aggressive low-power requirements.

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2. Contextualizing Shift-Left Methodologies in CTS and Voltage Scaling

One of the foundations of robust CTS-conscious voltage scaling is the increasing use of shift-left methodologies in Electronic Design Automation (EDA). These shift-left methods allow the identification of timing bottlenecks, power issues, and PVT variations at early stages of the design process. Such early observations are invaluable in developing CTS strategies that are sensitive to real operational dynamics rather than relying on post-layout patchwork solutions [1].

At sub-5nm nodes, design margins are very small. Therefore, there is a need to incorporate voltage scaling mechanisms directly into the CTS design process instead of treating them as post-synthesis alternatives. This integration can be achieved through shift-left approaches that test clock performance under different voltage conditions during early RTL development and physical synthesis stages. This time-sensitive alignment between design and power optimization helps ensure that voltage changes are not arbitrary, but are informed by actual timing analysis results, especially across worst-case distributed corners.

Furthermore, an extended form of shift-left involves tighter integration among design tools, enabling co-optimization between logic synthesis and placement, routing, and power management units. This unified approach is essential when introducing voltage scaling, as it must simultaneously address CTS limitations, placement density, thermal hotspots, and power grid integrity. Overall, shift-left paradigms align naturally with CTS-sensitive voltage scaling, as they promote an interconnected, timing-aware, and power-efficient design philosophy [1].

3. Test Optimization and Power Integrity in Sub-5nm Designs

This interaction between voltage scaling and design-for-test (DFT) optimization is becoming increasingly significant as voltage scaling becomes more tightly integrated into CTS strategies. At sub-5nm technology nodes, traditional DFT methods cannot be applied directly because transistors have become highly sensitive to PVT variations. Although the adoption of low operating voltages is beneficial for reducing dynamic power, it also introduces challenges such as maintaining uniform test vectors and the potential reduction in test coverage.

DFT optimization should therefore be a key consideration in CTS-conscious voltage scaling. Design methodologies must ensure that voltage scaling, while preserving clock integrity, does not lead to test escapes or reduced fault coverage. This requires finer-grained clock gating and careful scan chain timing, especially under scaled voltage conditions. Modern DFT approaches emphasize adaptive test strategies that are capable of self-calibrating using real-time voltage and timing data provided by the CTS framework [2].

Test compression and hierarchical test architectures offer viable opportunities in this context. Test patterns tailored to voltage islands can be used to partition the design into voltage domains, thereby enhancing test reliability. Additionally, embedded self-test (BIST) logic linked to CTS data can be incorporated, allowing continuous verification of clock performance across varying voltage levels. As a result, DFT is no longer an isolated verification stage but an active component of the overall power and timing management system in sub-5nm SoCs [2].

4. Voltage Scaling in Low-Power VLSI Design

Voltage scaling has been a key concept in low-power VLSI design. Nonetheless, the specifics of applying this method have changed significantly with the move to more advanced technology nodes. Below 5 nm, decreasing supply voltages can be offset by increased leakage currents and lower noise margins. Moreover, sensitive threshold voltage shifts and channel length modulation are caused by the aggressive reduction in transistor sizes.

With CTS-conscious voltage scaling, a more sophisticated way of addressing these challenges is adopted. This approach targets differential rather than uniform voltage scaling across the entire chip, synchronized with the temporal and spatial attributes of the clock tree. Technically, this implies that functional units farther from the clock source or located in thermal hotspots may be supplied with voltages different from those required by the timing characteristics of other functional blocks [3].

This fine-grained control helps preserve signal integrity while optimizing power consumption at a local level. For example, functional units with lower switching activity can operate at reduced voltages without violating setup or hold time requirements, provided their CTS paths are properly analyzed and tuned. Additionally, adaptive voltage scaling

schemes can respond to real-time workload variations and environmental conditions, dynamically adjusting supply voltages to achieve optimal performance per watt [3].

Table 1 Comparative Overview of Voltage Scaling Strategies

Voltage Scaling Strategy	Timing Sensitivity	Power Savings Potential	Implementation Complexity	CTS Integration
Static Voltage Scaling	Low	Moderate	Low	Minimal
Dynamic Voltage Scaling	Medium	High	High	Partial
CTS-Aware Voltage Scaling	High	Very High	Very High	Full

Source: Synthesized by author based on multiple references [1][2][3]

5. Area and Performance Considerations in CTS-Driven Voltage Scaling

The main trade-off of a CTS-aware voltage scaling implementation is its impact on chip area and performance. The physical design limitations of sub-5nm SoCs may require complex placement and routing layouts that can negatively affect clock assignment. When two or more voltage domains are involved, clock tree routing can become more complex in the presence of voltage scaling mechanisms. These issues require thorough analysis of area, power, and performance (PPA) metrics in the context of CTS.

From a layout perspective, implementing multiple voltage domains often requires isolation cells, level shifters, and sometimes redundant clock buffers to minimize skew and jitter. These components consume valuable silicon area and can increase both dynamic and leakage power. However, the resulting power savings and clock stability can offset these costs when appropriate CTS path matching and advanced physical design techniques are applied [4].

Such techniques include the use of advanced placement algorithms that optimally position logic blocks and co-optimize CTS buffer placement in a voltage-sensitive manner. By aligning voltage island boundaries with buffer insertion points, designers can minimize cumulative delays at voltage domain interfaces and reduce excessive buffering. Additionally, hierarchical CTS structures can be employed to simplify the management of distributed voltage domains and alleviate routing congestion commonly associated with complex clock networks [4].

Moreover, modern place-and-route tools that are CTS-aware can predict timing behavior across different voltage conditions. These tools leverage machine learning algorithms trained on historical design data to identify optimal trade-offs between area utilization and clock path integrity. This predictive capability not only simplifies physical implementation but also significantly improves post-silicon predictability, which is highly valuable at advanced technology nodes [4].

6. FinFET Innovations and Clock Performance Enhancement

As the physical limits of planar CMOS continue to be reached, FinFET technology has been introduced as a viable successor for continuing Moore's Law. Short-channel effects, electrostatic control, and drive strength have been enhanced by FinFET technologies. Of special interest in this context are the benefits they provide for CTS-conscious voltage scaling, in which the integrity of clock signals is of utmost importance.

The clock tree can be implemented using FinFET-based CMOS processes, which allow designers to achieve finer signal transitions, lower propagation delays, and improved noise resistance. These properties translate into more predictable clock behavior, which in turn enables more aggressive voltage scaling without violating setup or hold constraints. Additionally, the power-efficient nature of FinFET devices positively impacts the power-saving objectives of CTS-aware voltage management, particularly with respect to both dynamic and leakage power savings [5].

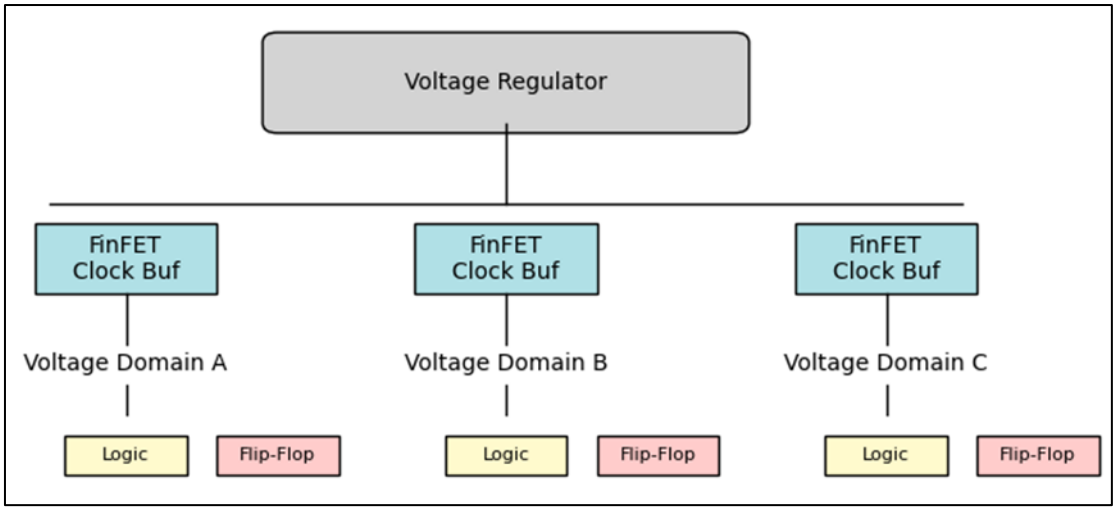

Figure 1 CTS-Aware Voltage Scaling with FinFET-Based Clock Buffers

Note: Diagram is illustrative and adapted based on content relevance. Proper CTS integration with voltage domains and FinFET buffers shown for clock robustness enhancement [5].

Furthermore, the scalability of FinFET technology can be used to design miniature, high-speed clock delivery systems that can be customized with extremely high precision to the timing needs of individual voltage domains. This granularity is of great importance in sub-5nm designs, where clock skew and jitter margins are essentially minimal. Therefore, the synergy between FinFET architecture and CTS-conscious voltage scaling is one of the pillars of the next generation of ultra-low-power SoCs [5].

7. Scaling Challenges in Heterogeneous Silicon Systems

System-on-Chip has evolved into a more specialized system with dedicated accelerators, analog blocks, and multiple voltage islands on a single die as semiconductor manufacturing processes move to sub-5nm fabrication. The timing characteristics and power input requirements of these components vary widely, making it difficult to centralize clock distribution. CTS-sensitive voltage scaling can be extended to such heterogeneity, allowing clock domains to be dynamically scaled to meet the needs of specific functional blocks while maintaining timing coherence at the macro level [6].

Interconnect latency and synchronization overhead are major bottlenecks in highly parallel systems, including those developed to support AI and data analytics workloads. Partial solutions such as asynchronous interfaces or hybrid synchronous–asynchronous architectures have been proposed, typically at the cost of more complex verification. CTS-sensitive strategies may provide a more refined solution by enabling voltage scaling across distributed corners of the die. This allows different regions of the SoC to operate at their optimal voltage and frequency ranges while maintaining global synchronization standards [6].

Scalable silicon platforms also require the clock tree itself to scale across a wide range of die sizes, shapes, and configurations. Hierarchical and mesh-based CTS structures are becoming increasingly popular, as they permit more effective clock distribution and voltage control. These methods provide local flexibility and global coordination, which is especially essential in chiplet-based designs or three-dimensional integrated designs [6].

8. Wireline Communication and Clock Timing Sensitivity

The impact of voltage scaling on high-speed communication links in SoCs is another dimension of the CTS domain that is often neglected. Wireline interfaces, including those using PAM4 modulation to enable operation over very long distances, are highly sensitive to jitter and bit error rate (BER). This sensitivity can be aggravated by voltage fluctuations within the clock domain, resulting in loss of data integrity and increased overhead from forward error correction or retransmissions.

These challenges can be mitigated through clock data recovery (CDR) circuits and feed-forward equalization (FFE) solutions that are closely coordinated with the CTS-conscious voltage management layer. FFE implementations based on maximum likelihood sequence detection (MLSD) have demonstrated that reducing computational complexity and minimizing BER are achievable only when underlying clock signals remain stable despite voltage changes [7]. This stability is directly related to how well CTS structures adapt to voltage variations across distributed corners of the die.

CTS-conscious voltage scaling architectures that are sensitive to wireline timing can dynamically adjust to ensure that jitter margins remain within acceptable limits. This may involve predictive scaling, where the system estimates load-induced clock delays and preemptively adjusts supply voltages, or reactive scaling, where load-induced jitter is detected through real-time monitoring and voltages are adjusted accordingly. In both cases, tight coordination between the CTS layer and voltage regulation logic is essential to maintain data fidelity in high-speed interfaces [7].

9. Variability and Reliability in Scaled MOSFETs

Scaling voltages in a CTS-aware fashion does not depend solely on architectural ingenuity; it also relies on the physical robustness of the underlying transistor designs. Deeply scaled MOSFETs face significant variability challenges, including random dopant fluctuations, line-end variations, and gate oxide thickness variations, all of which can unpredictably affect clock path timing. These issues are further aggravated by voltage scaling, which reduces noise margins and makes circuits more susceptible to timing errors [8].

The design of CTS-sensitive strategies should therefore account for these sources of variability. Adaptive biasing of clock path buffers and inverters, along with threshold voltage adjustment, is one mitigation approach. In this way, transistor-level and environmental variations can be dynamically corrected, ensuring that clock signals reach all destinations with acceptable skew and delay [8].

In addition, effective CTS design should incorporate comprehensive worst-case corner analysis across voltage and process variations. This goes beyond simulating only the fastest and slowest paths and includes more realistic intermediate scenarios that are likely to occur in practice. Insights from these simulations can be integrated into voltage scaling strategies, enabling the system to proactively adjust supply voltages or activate redundant paths when timing violations are detected [8].

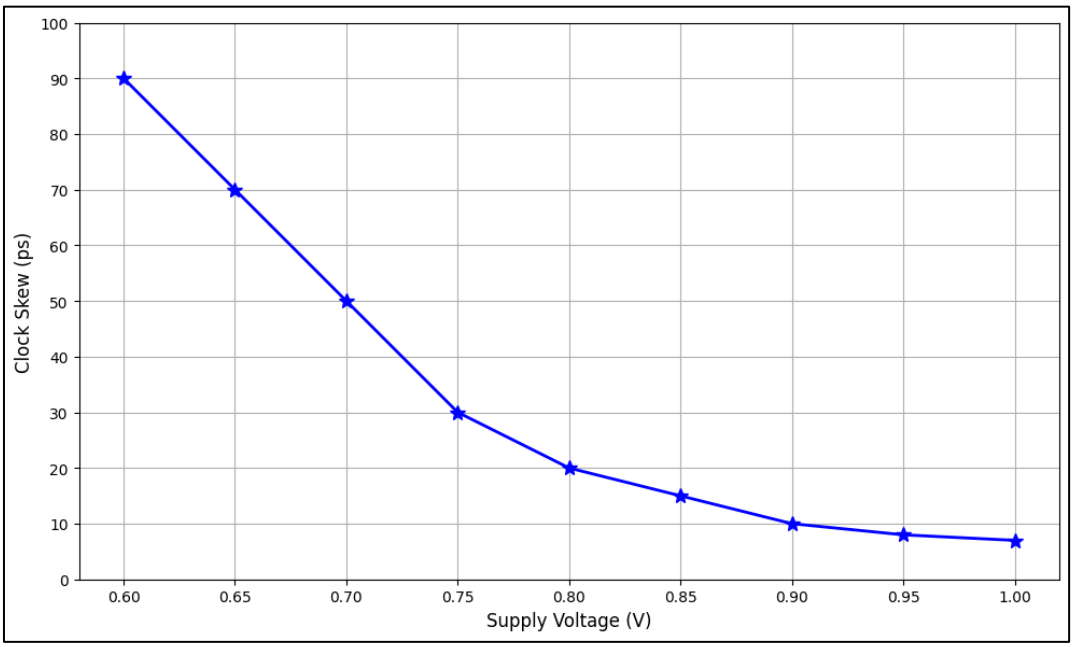

Figure 2 Impact of Voltage Scaling on Clock Skew Across Process Corners

Graph adapted and conceptualized from performance variability data in scaled MOSFETs [8]

As shown above, the non-linear relationship between voltage levels and clock skew highlights the importance of granular control in CTS-aware voltage scaling. Skew increases sharply as voltage drops below threshold, particularly in slower process corners, reinforcing the need for dynamic compensation mechanisms within the CTS framework.

10. Precision Nanofabrication and Clock Distribution Networks

The ability to accurately fabricate nanoscale features is a key capability that facilitates CTS-conscious voltage scaling strategies. Sub-5nm SoCs require extremely small routing, vias, and active device features to preserve consistent electrical properties. Even a single deviation in fabrication can introduce parasitic capacitance, resistance, or physical asymmetry in the clock distribution network, leading to timing imbalance.

Recent developments in single-crystal silicon–based fabrication technologies with high precision allow smaller feature sizes and greater regularity of clock paths. These advances enable the use of symmetrical H-tree or X-tree clock topologies, which are less vulnerable to routing-induced skew. Improved nanofabrication control reduces variability, which in turn simplifies voltage scaling mechanisms and makes CTS integration more predictable [9].

Moreover, enhanced lithography and etching methods ensure a higher degree of correspondence among buffer features across the chip. This is particularly important in CTS-aware scaling, where voltage-induced changes in one section of the clock tree should not propagate to other sections of the network. Finer fabrication reduces the need for overdesign and guard-banding, minimizes wasted area, and lowers power slack, thereby improving overall efficiency [9].

11. Device-Level Optimizations for Sub-5nm CTS Paths

At the device level, new transistor architectures are being investigated to further improve the feasibility of CTS-aware voltage scaling. One such example is the spacer-engineered Junctionless FishBone (JL-FB) FET, which is designed to offer better electrostatic control and lower subthreshold leakage than older device structures. These transistors can operate at reduced voltages along CTS paths without compromising switching speed or drive strength [10].

This advantage arises from the unique geometry of the JL-FB FET, which produces a smoother electric field and, consequently, more predictable gate delay. Such predictability is essential for CTS paths, where variations on the order of a few picoseconds can lead to functional errors. In addition, these devices enable clock networks to reduce power consumption without affecting performance integrity [10].

Another key distinction of the JL-FB FET is its compatibility with complex back-end-of-line (BEOL) processes, allowing it to be integrated into densely populated standard-cell libraries with minimal design-rule trade-offs. This compatibility supports its practical use in sub-5nm SoCs, where maintaining clock integrity and power efficiency is of critical importance.

12. Conclusion

CTS-conscious voltage scaling is one of the key breakthroughs in the design and optimization of sub-5nm System-on-Chip architectures. It is claimed to deliver significant power savings, improved clock resilience, and enhanced timing reliability by aligning power management operations with clock distribution complexities. Shift-left methodologies are integrated to ensure that timing and voltage dependencies are considered as early as possible in the design process, thereby reducing late-stage surprises and improving design closure.

Other innovations that contribute to the benefits of CTS-aware voltage scaling include FinFET technologies, scalable silicon platforms, and high-precision nanofabrication. These advancements enable more precise manipulation of voltage and timing parameters, with particular attention to distributed corners of the die where uniform scaling is no longer effective. In addition, emerging device technologies such as JL-FB FETs further support the development of robust clock networks capable of operating reliably under aggressive voltage scaling conditions.

CTS-aware voltage scaling is therefore a critical enabler as semiconductor design moves toward greater heterogeneity, higher performance, and lower power consumption. It helps the industry address increasing clock distribution complexity while achieving broader goals of energy efficiency, scalability, and reliability in next-generation SoCs.

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